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## Power Integrity Analysis of DDR2 Memory Systems during Simultaneous Switching Events

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## Abstract

Simultaneous switching noise (SSN) in systems using single ended drivers poses significant design challenges as data rates continue to increase. In this paper, we analyze the impact of SSN on a DDR2 memory system using a wire-bond package for the controller and operating at 667MHz. We not only focus our attention on the supply rail where the output driver is located, but also on the other supply rails where sensitive circuits are located. We demonstrate that the noise coupled into these sensitive supply rails through either other supply rails or signals can be significant. In addition, we present a methodology for finding data patterns that cause the worst case supply noise on each supply rail. Finally, the simulated supply noise is correlated with hardware measurements to validate the modeling approach.

## Authors Biography

Ralf Schmitt received his Ph.D. in Electrical Engineering from the Technical University of Berlin, Germany. Since 2002, he is with Rambus Inc, Los Altos, California, where he is an engineering manager responsible for power integrity on chip, package, and system level. His professional interests include on-chip signal integrity, power integrity, timing analysis, clock distribution, and high-speed digital circuit design.

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Woopoung Kim studied his Ph.D degree in Electrical Engineering at Georgia Institute of Technology, Atlanta, GA USA, in 2004 where he developed a transmission

line model, called non-physical RLGC models, for high-speed system simulations. He joined Rambus Inc., Los Altos, CA USA, in 2004 where he has been involved in signal-integrity/ power-integrity research for high-speed I/O's.

Dan Oh is Engineering Manager at Rambus Inc. He is currently responsible for the signal integrity analysis and design related with memory interface products. Previously, he was a developer at Synopsys where he implemented several signal integrity features in Hspice and other on-chip parasitic extraction tools. Dr. Oh received his Ph.D. degree from the Department of Electrical and Computer Engineering, University of Illinois at Urbana-Champaign in 1996. His professional interests include high-speed signal modeling and design.

## I. Introduction

Today's computing systems require ever increasing bandwidth even for cost-sensitive consumer applications such as HDTV. The bandwidth requirements in these systems are reaching levels previously associated with high-performance workstations, servers, and routers. At the same time, cost is a major design factor for these systems. Therefore, there is a great interest in implementing high-speed interfaces using low-cost technologies such as wire-bond packages.

The data rate of DDR2 systems is expected to move from currently 400MHz to 667MHz and 800MHz in the near future. At these high data rates, jitter introduced by supply noise can significantly reduce the timing margin in the system. As typical for interface systems using single-ended signaling, DDR2 memory systems can generate substantial current peaks when output drivers are switching simultaneously. These current peaks in return generate supply noise (SSN) in the system if the impedance of the power distribution system is not sufficiently low. In particular, many systems using DDR2 memory interfaces are implemented using limited silicon area for on-chip bypass capacitors and packages using wire-bond technology. Wire-bond packages typically add a substantial amount of inductance to the power distribution network (PDN), resulting in a large impedance of the power distribution system around the package/chip resonance frequency. As a result, there is a significant amount of supply noise in the system by design, especially on the power rails used for output buffers. A way to address this problem is moving noise sensitive circuits away from the noisy buffer supply. Additional supply rails are introduced for supply noise sensitive circuits like PLLs and clock drivers, in an effort to minimize the jitter caused by supply noise. During SSN events, the current dissipation on these rails usually does not change directly. However, noise can be generated on these rails by coupling between bond wires of different rails, by coupling between signal wires and supply wires, and by ground bounce on the shared ground rail. This coupled noise often has significant impact on the device jitter during SSN events in addition to the noise on the output driver supply rail itself. Therefore, predicting the SSN leading to jitter in the interface requires a power distribution model that includes these sensitive supply rails in the model and accounts for all coupling mechanisms into these rails.

In this paper we present a methodology to accurately model the supply noise of a 667MHz DDR2 during SSN events. First, a model for the power distribution system of the interface is presented which addresses self-induced noise as well as coupled noise on all supply rails. Next, the dependency of each noise component to the data pattern transmitted in the interface is discussed and worst-case access profiles are derived. Finally, simulation results of supply noise and jitter profile on a test system are compared to measurements, showing correlations with good accuracy. Amplitude as well as waveform of supply noise simulated on different rails and for different access patterns in the interface are confirmed by measurements with an accuracy of few percent. Measurements of jitter sensitivity to local bonding implementations are correlated to noise coupling simulation results, confirming the accuracy of the noise coupling model and emphasizing the importance to include noise coupling into the SSN analysis.

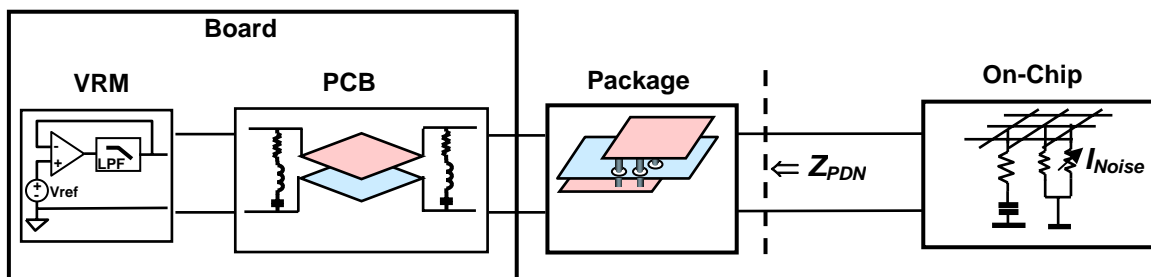
## II. Supply Noise Modeling Methodology for Interface Systems

### II.1. General System Level Power Distribution Models

High-speed interface systems require high quality power supply systems. Power and ground bounce on the supply rails causes signal distortion, affects timing and noise margin, and introduces jitter. As the data rate of interfaces increases, the acceptable timing loss due to supply distortion is decreasing.

Self-induced supply noise is generated when the current dissipated in the system changes over time. Interface systems, in particular I/O systems using single-ended signaling schemes, are causing current changes at every signal transition. A major challenge for the power distribution system is simultaneous switching events, when many interface signals are switching at the same time causing severe current changes in the system. In order to limit the supply voltage fluctuations caused by these current changes, the impedance of the power distribution network (PDN) seen by the interface circuits has to be low over a wide frequency range.

It was shown in [1] that modeling the impedance of the power distribution network over the entire frequency range of interest requires a model covering several levels of the design hierarchy. *Fig. 1* shows the schematic of a power distribution model for the supply rails used for internal circuits. It models the impedance  $Z_{PDN}$  of the power distribution system at low and medium frequency, which is the frequency range most interesting for simultaneous switching events.



*Fig. 1: Schematic of PDN for internal supply rails at low and medium frequency*

The impedance  $Z_{PDN}$  seen between the supply voltage and ground by the circuits on the silicon is dominated by components on different system hierarchy levels at different frequencies. At high frequencies, the on-chip distribution system and the package are dominating, while at very low voltages the Voltage Regulator Module and decoupling capacitors on the PCB are determining  $Z_{PDN}$ . The profile of  $Z_{PDN}$  over the frequency range of interest is used as a Figure-of-Merit for the power distribution system.

### II.2. Power Distribution Model for Interface Systems

A concept widely used in the design of power distribution systems is the ‘target impedance concept’. The design methodology in this concept is to keep the power

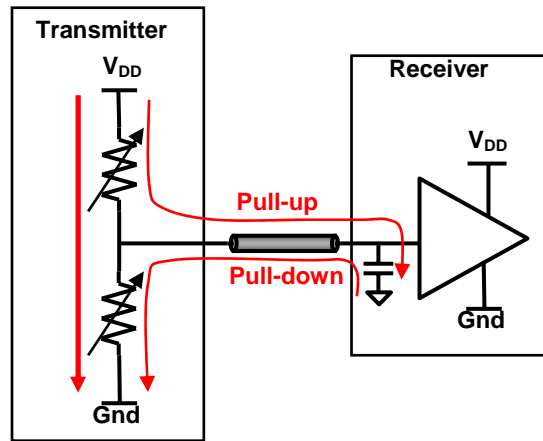
distribution impedance  $Z_{PDN}$  below a target impedance  $Z_{target}$  over the entire frequency range of interest. The target impedance  $Z_{target}$  is calculated as:

$$Z_{PDN}(f) \leq Z_{target}(f) = \frac{V_{Noise}(f)}{I_{Noise}(f)}$$

where  $V_{Noise}$  is the allowed voltage noise and  $I_{Noise}$  is the supply current change causing the noise.

In this concept it is commonly assumed that the supply noise current  $I_{Noise}$  is flowing between the power supply node and the ground node. Therefore, the impedance  $Z_{PDN}$  is defined between the supply nodes at the interface between package and chip, as shown in *Fig. 1*. For supply rails providing power to internal circuits this is a reasonable assumption for the average currents of larger circuit blocks, even if it is incorrect for an individual logic gate. In CMOS technology, e.g. the current is flowing during pull-up from the positive supply ( $V_{DD}$ ) to an internal capacitance at the output node, and at a later time during pull-down from the internal capacitance to the negative ( $V_{SS}$ ) node. Strictly speaking, therefore, the gate current is not flowing directly between  $V_{DD}$  and  $V_{SS}$ . However, for a larger circuit block the superposition of pull-up and pull-down currents of many gates appears as a direct current between the supply rails  $V_{DD}$  and  $V_{SS}$ .

For interface systems, the assumption that the current flow is mainly between the supply rail (e.g.  $V_{DD}$ ) and ground is not true anymore. As an example, *Fig. 2* shows the schematic of an interface using voltage-mode signaling. In such an interface, the main current components will often still be flowing directly between the supply rail and ground, since both pull-up and pull-down path are conducting typically at least temporarily during transitions. Additional current components, however, will charge the external load capacitance from the supply voltage  $V_{DD}$  during pull-up and discharge this capacitance to ground at a later time during pull-down.



*Fig. 2: Current Components in Interface using Voltage-Mode Signaling*

Even if both charging and discharging current are occurring with the same frequency, the response of the power distribution system to these two excitations cannot be described by the single PDN impedance  $Z_{PDN}$  defined in *Fig. 1* due to the phase shift between charging and discharging currents in the package and PCB supply. In order to

accurately model the current flow during switching operations the signal traces and the load capacitances have to be added to the PDN model of the transmitter. Neglecting these elements in an SSN analysis introduces errors into the analysis, over-estimating the supply noise during SSN events. But as long as the direct current between the supply rails of the transmitter dominates the total switching current, the resulting accuracy is often sufficient.

This is not true any more, however, for modern high-speed interfaces like DDR2, which are using current mode signaling. Fig. 3 shows an example of an interface using current-mode signaling.

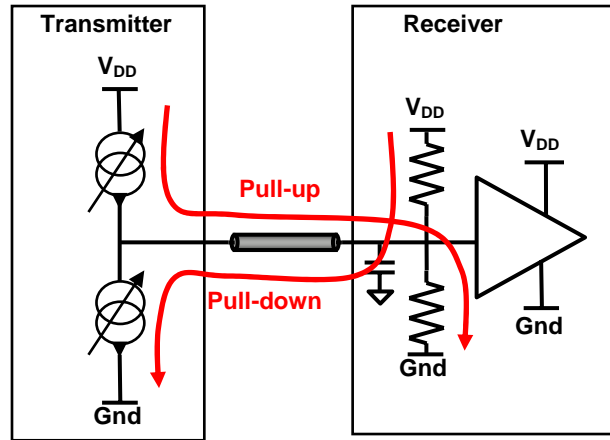


Fig. 3: Current Components in Interface using Current-Mode Signaling and On-Die Termination

In current mode signaling, the major current components are flowing between one supply rail of the transmitter and load resistors at the end of the signal channel. These load resistors can be either on the receiver chip or on the PCB. In both cases, in order to model the current flow during switching operations it is necessary to add the signal channel and the load resistor to the power distribution model.

Thus, in order to model SSN noise in a high-speed interface, it is necessary to combine the model of the power distribution network of both the transmitter and receiver with a model of the signal traces in the system. This has the additional advantage that noise coupling between signal traces and the supply network can also be modeled in the same model. A simple model of the power distribution of e.g. the transmitter alone is not sufficient, as it does not model the current distribution in the system correctly during switching operation.

Since there are multiple current loops in the system contributing to supply noise in the system, it is also not possible anymore to define a single power supply impedance  $Z_{PDN}$ . At least, separate target impedances have to be defined for each current loop in the system.

There is a further limitation of the target impedance concept that limits its usability for the design of interface systems. The target impedance concept assumes that the worst-case current excitation can be modeled as a single-frequency excitation. In this case, the

supply noise amplitude can be calculated as product of noise current amplitude and power distribution impedance:

$$V_{noise} = Z_{PDN} \cdot I_{noise}$$

If for a given frequency range the acceptable voltage noise amplitude  $V_{noise}$  and a maximum, single frequency AC current excitation  $I_{noise}$ , are known, then a single value  $Z_{target}$  can be calculated for this frequency range.  $Z_{target}$  can be a function of frequency, as the acceptable voltage noise amplitude changes over frequency or if the maximum possible (single frequency) current excitation varies with frequency. However, the target impedance concept is not well suited for cases with largely distributed  $I_{noise}$  spectrum, where noise contributions at different frequencies are superimposing. This is the typical case for interface systems, where current component contributions at different frequencies and phase relationships are superimposing. In these cases it would be possible to calculate the supply noise contribution of each of these spectral components and add them together. However, this is very pessimistic, since it ignores the phase relationship between the different components. Therefore,  $Z_{PDN}$  can be used for these cases as a relative 'Figure-of-Merit' to compare different implementations and identify critical frequencies. For final supply noise verification, however, a simulation in time domain is required, which naturally considers the phase relationship of the noise contributions.

### 11.3. Self-Induced and Coupled Noise in Interface Systems

The goal of our SSN analysis for interface systems is predicting the margin loss in the system due to the simultaneous switching of output drivers. Often, SSN analysis focuses on the self-induced supply noise on the output driver supply rails, i.e. the noise generated by the output drivers on their supply rails during switching. The sensitivity of most single-ended drivers to noise on their supply rails, however, is usually not severe. Thus, this self-induced noise component often has only limited impact on the timing and voltage margin of the interface system. In contrast, noise on supply rails not used by the output drivers, but used for sensitive circuits like PLLs and clock drivers, can have a much larger impact on system jitter. Therefore, supply noise generated on these sensitive supply rails during simultaneous switching events has to be included into the SSN analysis in order to predict the system margin loss during these events.

There are three major sources for noise coupling into internal supply rails other than the buffer supplies during simultaneous switching events. The first source is signal-to-supply coupling in package and PCB. This noise coupling can easily occur in wire-bond packages. Modeling this noise coupling requires a package model that reflects the coupling between individual bond wires. It also requires that all signal lines are excited with worst-case pattern to excite the largest noise amplitude in the sensitive supply rail.

The second source of coupled noise into internal supply rails is supply-to-supply coupling from the output driver rails in package and PCB. Similar to the signal-to-supply coupling, wire-bond packages can easily couple noise between the driver supply rails, which experience large current surges during simultaneous switching events, and bond wires of sensitive supply rails. Additionally, supply noise can be coupled between the supply rails on the PCB, especially if both supply rails are sharing the same regulator on the PCB. In this case, the PCB supply and any filter between the different supply rails have to be included in the SSN simulation model.

The third source of coupled noise into internal supply rails is ground bounce on shared  $V_{SS}$  nodes inside the chip. The inductance of the ground distribution, especially in the package, causes ground bounce during simultaneous switching events that change the voltage difference between the internal supply rail and the shared ground rail. Another source of ground bounce is the voltage drop on the highly resistive on-chip power distribution (IR drop). As the activity in the circuits on the chip is changing, the distribution of IR drop over the chip is changing as well.

Thus, simulating the noise coupled into internal supply rails other than the buffer supply during simultaneous switching events requires a complete model of the driver supply, the internal supply, and the entire signal channel all at the same time.

#### 11.4. Driver Model for SSN Analysis

The simulation of supply noise under simultaneous switching conditions requires an accurate model of the power distribution network under switching conditions as well as accurate current profiles exciting this network.

Ideally, accurate transistor-level transmitter and receiver models could be used for the SSN simulation. These transmitter and receiver models naturally provide accurate current profiles on the supply rails, including feedback effects due to rail collapse. They also provide accurate waveforms on the signal lines modeled in the PDN system, and thus allow modeling the coupling between signal and supply traces. Furthermore, combining the power distribution model with the channel model and using the full transistor-level driver and receiver models allows simulating the impact of supply noise on the signal timing. The disadvantage of full-transistor driver and receiver models is the large complexity of these models. Common analog simulation engines like Spice are only able to simulate interfaces with a small number of signal lines using transistor-level transmitter and receiver models. Larger interfaces require simplified transmitter and receiver models that can be simulated more efficiently.

IBIS models are simple receiver models commonly used for signal integrity simulations. These models are very efficient to simulate, so, analyzing a large interface is easily possible. However, common IBIS models don't provide accurate supply current waveforms and don't include the impact of SSN noise on the internal power rail ([2]). There are currently activities to improve the current profile accuracy of IBIS models (e.g. [3]), but even with these extensions only some of the interactions between supply noise and current profile are modeled and accuracy of the resulting current profiles is still a concern.

An elegant way to achieve transistor-level accuracy with limited complexity is using Current Controlled Current Sources (CCCS) to duplicate the current profiles of one or a few accurate drivers. In this approach, a single driver is implemented using a transistor-level accurate model. The current profiles at all supply and signal ports of this 'master' driver are measured and duplicated to the corresponding position of other drivers. This creates correct current profiles on the supply net, identical to the current profile expected if all drivers were implemented using transistor-level models, and also accurate waveforms on the signal lines. This approach also preserves the feedback of rail collapse on the drivers, as the 'master' driver experiences the full supply noise caused by all drivers at the same time, reflecting the effect of rail collapse in its port currents. It is also

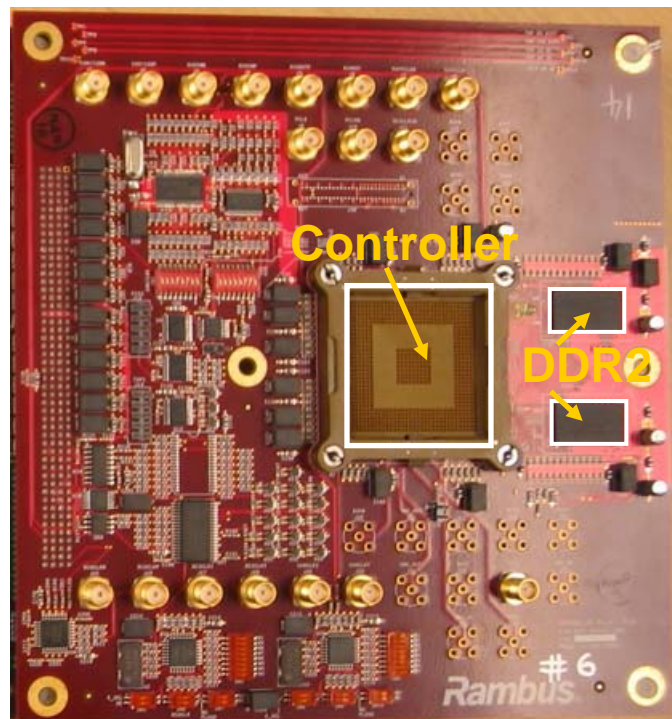
very computationally effective, since CCCS elements require very little simulation effort for an analog simulator like Spice.

Duplicating port currents with CCCS circuits requires that the port impedances of the 'master' driver is identical with the port impedances of the duplicated drivers. For the supply ports this is usually the case, since all drivers share the same power distribution environment. For signal lines, the reflection behavior of signal lines with CCCS based duplicated drivers should be identical to the reflection behavior seen by the 'master' driver. In systems with well terminated signal buses this is easily achieved.

If different signal lines are operating at different frequencies or with different data patterns, separate 'master' drivers are needed for each frequency or pattern. Even in this case, large interface systems can be easily modeled with a small number of transistor-level models, limiting the complexity of the interface model.

### III. SSN Model for DDR2 Test System

Fig. 4 shows a picture of the DDR2 test system analyzed in this paper. A detailed description of the system can be found in [4]. The system consists of one DDR2 controller and a single rank of two x16 DDR2 devices, operating at 667 MHz. The DDR2 interface consists of 32 data signals operating at a data rate of 667 MHz and 21 address and control signals operating at half the data signal rate.



*Fig. 4: DDR2 Test System Board*

The system is implemented on a 6 layer PCB board. The controller uses a wire-bond package demonstrating that DDR2 interfaces of this data rate can be implemented in a low-cost package system. The interface in the controller chip uses power supply rails that

are separated from the power supply of the ASIC core. All power supply rails use individual voltage regulators to prevent noise coupling on the PCB board.

The controller DDR2 interface uses the supply rail VddIO of 1.8V for output drivers, and the supply rail Vddr of 1.2V for other circuits in the interface. Both supply rails share a common ground node V<sub>SS</sub>. Fig. 5 shows the power delivery model of the data bus of the interface system. A similar model was added for the address/control bus of the system.

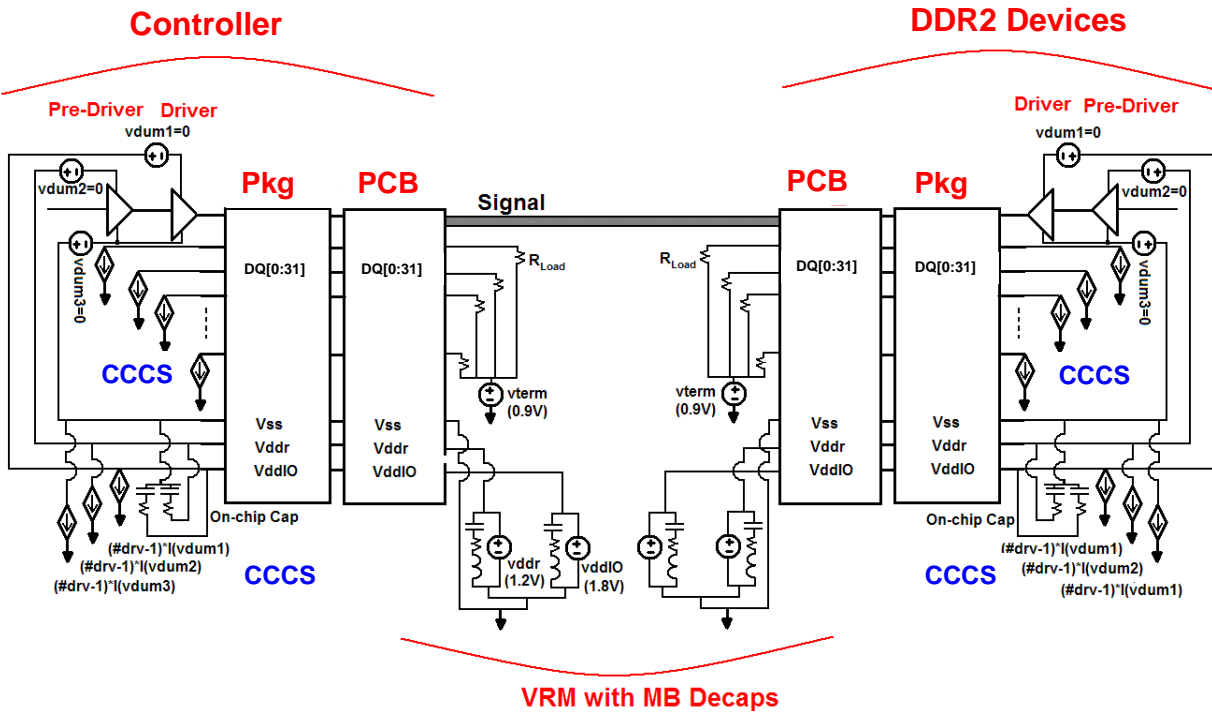


Fig. 5: Power Supply Model of DDR2 Data Bus for SSN Analysis

The SSN model shown in Fig. 5 allows simulating supply noise inside the controller as well as inside the DDR2 device during ‘read’ and ‘write’ operations. In the scope of this work we will focus on the supply noise inside the controller, as we verify the controller design. Few details were available about the package and on-chip supply network of the DDR2 device. Therefore, simplified models of the package and the on-chip power distribution of the DDR2 devices were used in this analysis. This has little impact on the noise simulations for supply rails inside the controller, but makes noise simulations inside the DDR2 devices less accurate.

Special attention was given to the package model of the controller. Wire-bond packages add a substantial amount of inductance to the supply network. In many cases, the impedance of the supply loops is dominated by the inductance of the bond wires in the package. Furthermore, coupling between bond wires are a major source of signal-to-supply and supply-to-supply coupling in the system. Therefore, a 3-D field solver was used to extract a package model from a 3-dimensional picture of the entire wire-bond section of the package based on the partial inductance concept. This model preserves the

inductive coupling between all bond wires. Additional traces and planes in the package can be added using conventional modeling methodologies like presented in [1].

*Fig. 5* shows a single transistor-level driver and receiver circuit for the data bus of the system. The remaining 31 data lines are excited using CCCS current mirrors. This configuration requires that all data signals are transmitting the same data pattern. If groups of signal lines are required at different frequency or data pattern, additional transistor-level driver and receiver models are necessary. For SSN analysis this is typically not the case, since the largest current excitation is achieved if all drivers are switching at the same time.

The address/control bus of the system, which is not shown in *Fig. 5*, operates at half the frequency of the data bus. The characteristic impedance and termination of address/control transmission lines is also different from data bus lines ([4]). Therefore, implementing the address/control bus requires an additional transistor-level driver.

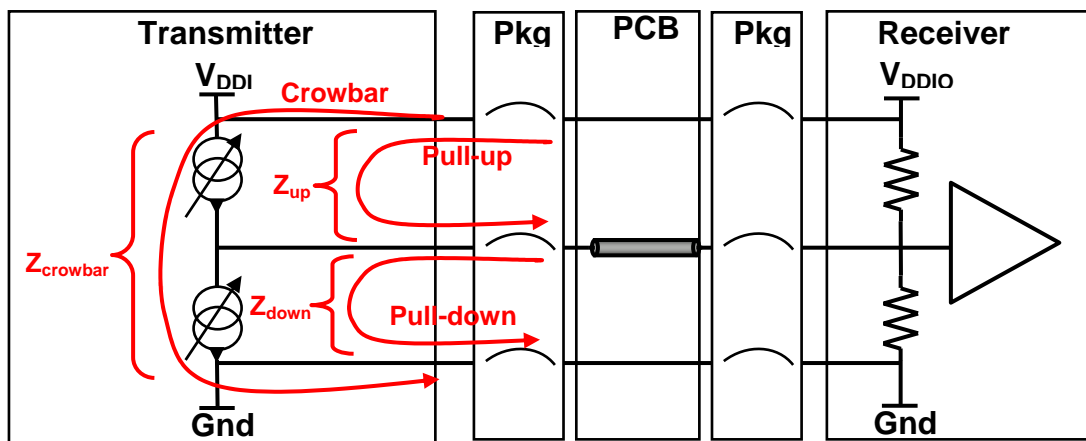
## IV. Determining Worst-Case Switching Profiles

Supply noise in a system is generated as a reaction of the supply network to current changes in the system. The amplitude of the supply noise generated by a (single frequency) current excitation is dependent on the impedance of the supply network at that frequency. Larger supply noise amplitudes are created when current changes excite the power delivery system at frequencies of high power supply impedance. A common way to find worst-case excitation pattern in a system is analyzing the power distribution impedance profile  $Z_{PDN}(f)$  and identifying excitation pattern that cause large current spectral components at frequencies of high  $Z_{PDN}(f)$  ([5]).

In interface system, finding the worst-case excitation to create the largest system jitter is more complicated, as the system is described by more than one power supply impedance, and each of these impedances can have different profiles over frequency.

### IV.1. Worst-Case Access Pattern for Self-Induced Noise

*Fig. 6* shows the current flow in the system during different stages of switching activity at the output drivers.



*Fig. 6: Current Flow During Different Stages of Output Driver Switching*

During pull-up, the current is flowing through the transmitter from the VddIO supply rail to the signal lines. The impedance of this current loop, as seen by the transmitter circuits, is  $Z_{up}$ . Similarly, the impedance  $Z_{down}$  is the supply impedance seen by the transmitter during pull-down operation. For the crowbar current, which is flowing while both the pull-up and the pull-down path of the output driver are active, the supply impedance is  $Z_{crowbar}$ , which is the ‘traditional’  $Z_{PDN}$  between VddIO and Gnd. All three current loops contribute to the total supply noise in the system. In order to identify the worst-case activity pattern in the system, all three impedances, have to be analyzed. Fig. 7 shows the impedance profiles of  $Z_{up}$ ,  $Z_{down}$ , and  $Z_{crowbar}$  for the test system.

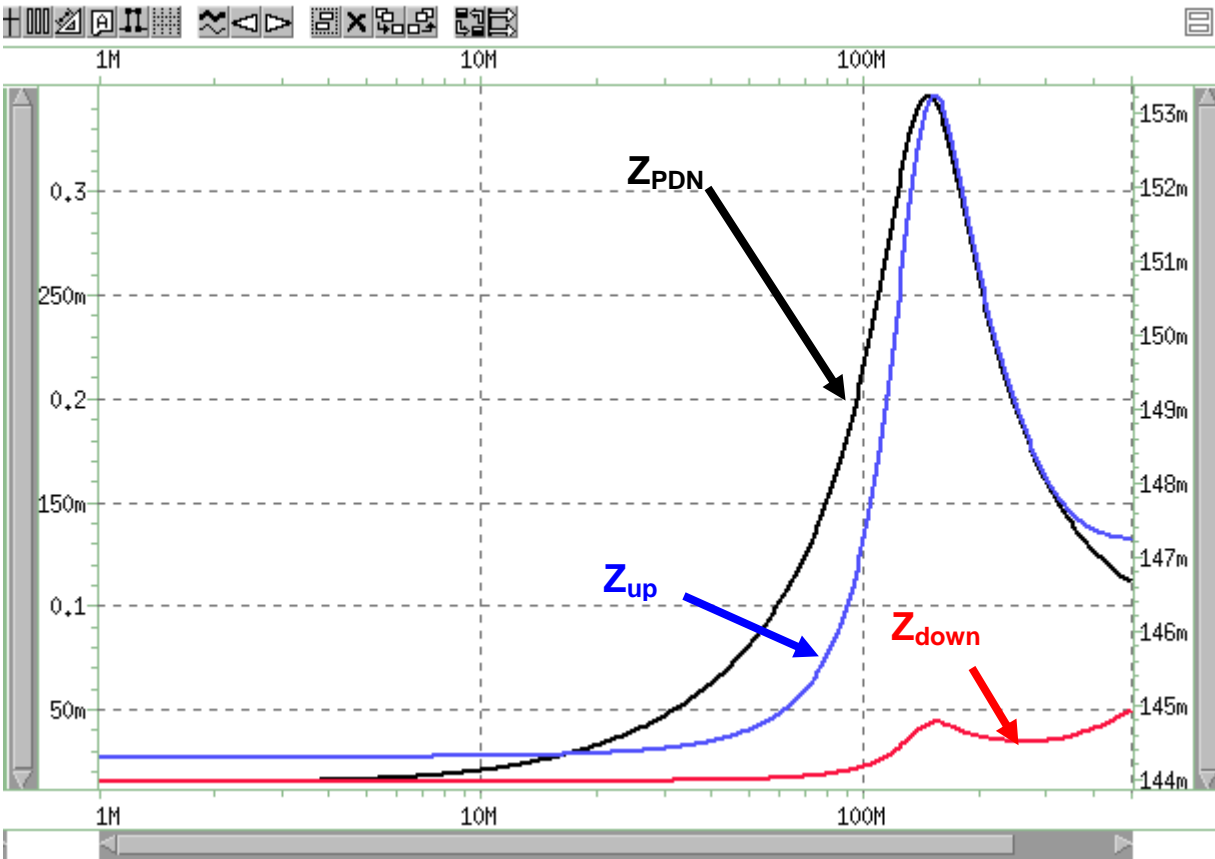


Fig. 7: Impedance Profiles for Self-Induced Noise on Output Driver Supply Rail

Fig. 7 shows that in our test system all three supply impedances have maxima at approximately the same frequency of approximately 150MHz. Assuming that all noise contributions superimpose with worst-case phase offset, maximum noise amplitude on (VddIO-Vss) is expected for data pattern creating large current components at this frequency. Dependent on the phase offset between the different noise components, however, patterns at a slightly different frequency can result in even worse supply noise. Therefore, several patterns with current frequencies close to the frequency of maximum supply impedance will have to be tested using time-domain simulations.

In a DDR2 system operating at a data rate of 667MHz, a pattern of 1100... on the data lines will cause current excitations at 167MHz, which is close the frequency of maximum supply impedances. The address/control signals, operating at half the data rate, will create current excitation at the same frequency when transmitting a pattern of 1010... .

#### IV.2. Worst-Case access pattern for Coupled Noise

In order to analyze the sensitivity of the system to couple noise into another supply rail, we again have to analyze the impedance seen between supply noise and current exciting the noise. This time, however, this impedance is the transfer impedance, not the self-impedance, between the voltage noise created in the internal supply rail and the current excitation on another supply rail or signal line causing this noise. This makes the process to find the worst-case excitation for coupled noise very similar to the same process for self-induced noise. It also creates the same difficulties in interface systems: there are several possible contributions causing noise coupling, and each of these contributions requires different worst-case access pattern in the system. On top of this, self-induced noise on these internal supply rails has to be considered as well, especially if it is correlated to the activity of the output drivers. This is for example the case if a pre-driver is operating from the internal supply rail. Fig. 8 shows the different transfer impedances for noise coupling into the Vddr supply rail as well as the impedance of Vddr-Vss for self-induced noise.

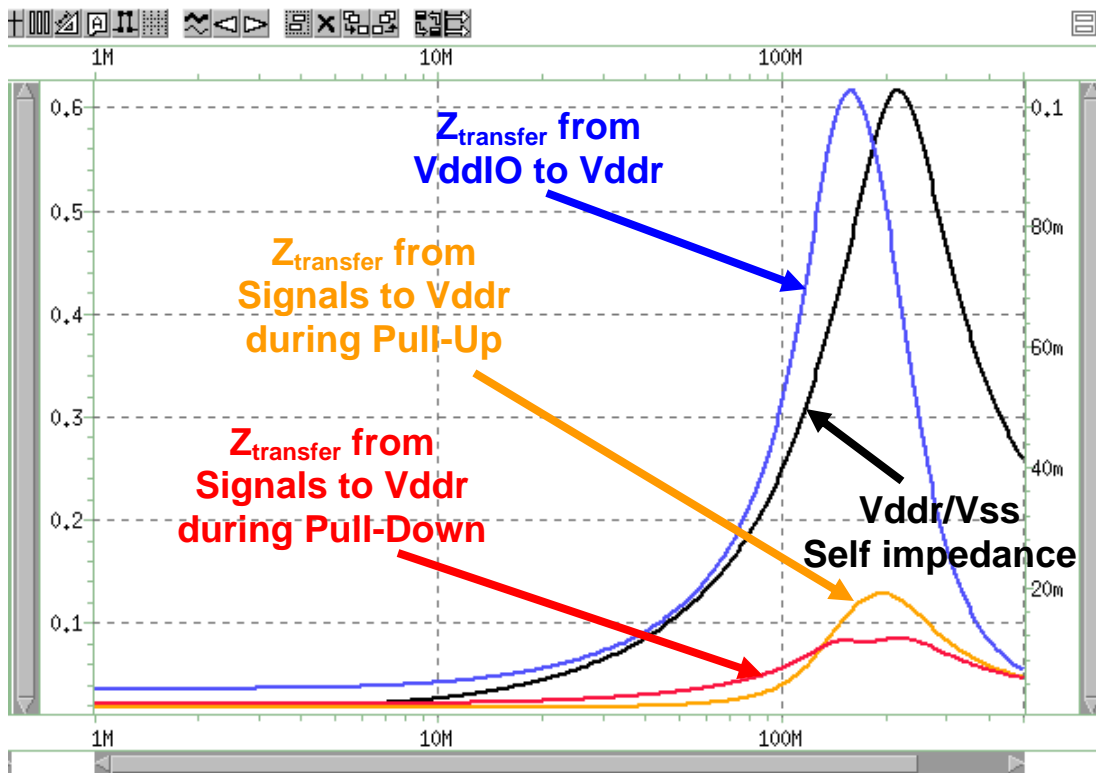


Fig. 8: Self- and transfer impedance for supply noise generation on VddR

In order to maximize the contributions of all components, the system would have to be excited at different frequencies for pull-up, pull-down, and crowbar operation. This is not possible, however, since the cycle time is always the sum of high and low time of the data sequence, and as such it is the same for all noise contributions. The noise amplitude will depend on the amplitude of each contribution, but also on the phase relationship between the contributions. Thus, it is not possible to determine a single worst-case excitation sequence from the AC analysis of the supply impedances any more. There are several patterns possible to be ‘worst-case’, and these patterns will have to be tested using a time-domain simulation. The ‘worst-case’ excitation, however, is still expected at a frequency where all supply impedances have larger impedance values, i.e. at frequencies between 150MHz and 230MHz. Thus, the AC analysis determines a frequency range where supply noise can be easily be generated. The final noise amplitude for pattern exciting this frequency range, however, has to be determined using time-domain simulations.

## V. Correlating Supply Noise Measurements

### V.1. Overview of Verification System

Simulations using the SSN analysis model were correlated with measurements on the test system shown in *Fig. 4*. This test system was designed as a verification system. As such, it was designed to provide access to data and address/control lines for signal and power integrity measurements.

The ASIC core of the controller chip provided full control over all data pattern transmitted on either the data or the address/control signal lines. In this way it was possible to send well-defined worst-case pattern over every signal lines, even if these pattern would not be possible in a real system due to the communication protocol on the control bus of a DDR2 system. As a result, the measured supply noise is more pessimistic than can be expected at normal operation, since a real system would not be able to excite the worst pattern sequence continuously on all signal lines. The measured noise, however, is an upper limit of the supply noise possible in the system under any operating conditions.

### V.2. Measuring Supply Noise on Driver Supply Voltage

The supply noise on the supply rails of the output drivers can be directly measured at the output of one driver. A detailed description of this measurement methodology can be found in [5]. During this measurement, one driver is transmitting a constant value, either ‘1’ or ‘0’, while all other drivers are transmitting the same worst-case data pattern. As long as the driver is transmitting a constant ‘1’, the driver supply rail VddIO is connected to the output signal through the on-die termination resistor of this driver. Any noise on the VddIO supply rail is reflected as noise on the signal line. The on-die termination resistor of the driver used for noise sensing can be added to the SSN simulation and correlated with measurements at the same location. The model then allows estimating the supply noise signal at the supply rail itself.

*Fig. 9* shows the signal measured at a data line of an output driver that transmitted a long string of ‘0’ followed by a long string of ‘1’ while all other drivers were transmitting

worst-case pattern. The measurement shows the supply noise on the VddIO and Gnd rails separately. During pull-up operation the output is connected to the VddIO rail, while during pull-down operation the signal is connected to the ground node. It can be seen that the nose on both rails is comparable in amplitude.

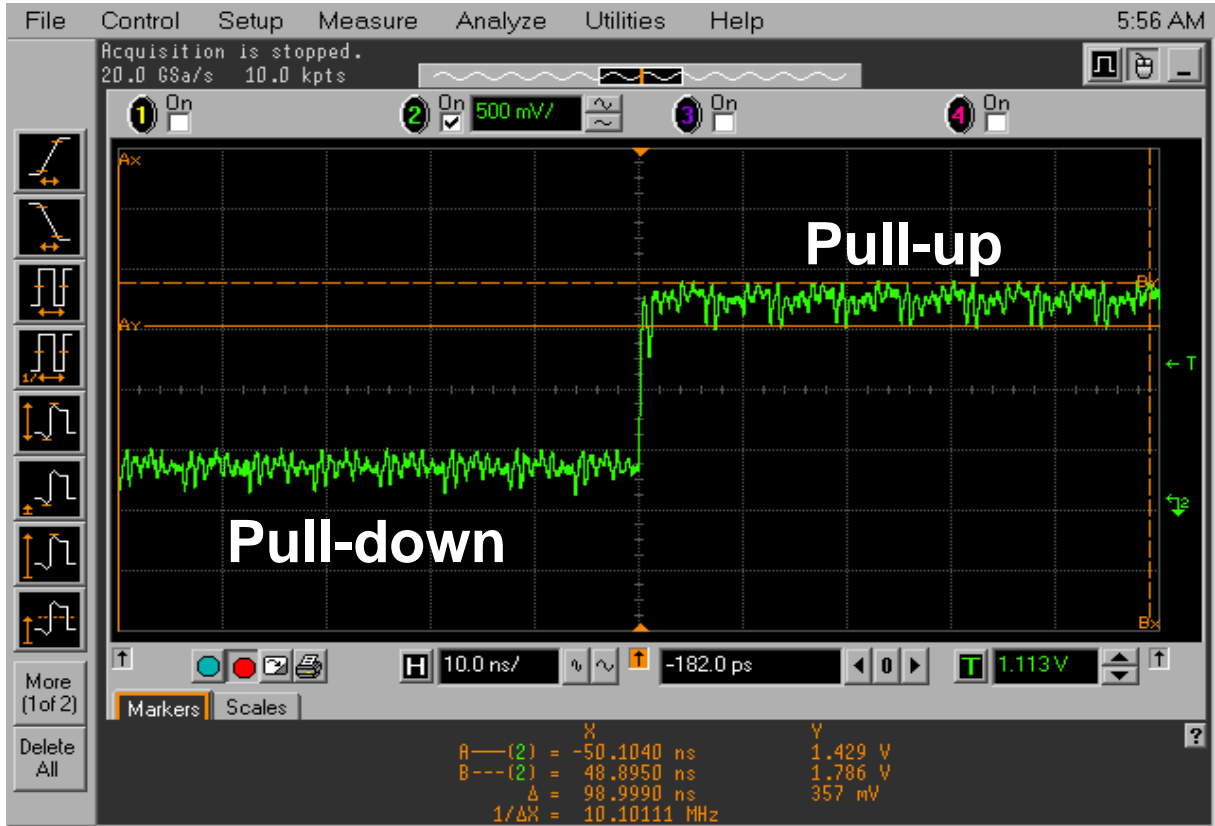


Fig. 9: VddIO and Gnd Supply Noise Measurement at Driver Output

The following table lists two of the data sequences used for supply noise correlation. The table also lists the dominating current excitation frequency generated by these sequences for a data rate of 667MHz. These sequences were chosen based on the supply impedance analysis described earlier. The current excitation frequencies generated by these sequences are close the frequencies where the different supply impedances approach their maximum values.

Name	Data bus signals		Address/control signals	
	Sequence	Frequency	Sequence	Frequency
Pattern 1	1100	167MHz	1010	167MHz
Pattern 2	110	222MHz	1010	167MHz

Since the address/control bus is operating with half the data rate in a DDR2 design, the maximum frequency achievable on address/control lines is 167MHz for a data rate of 667MHz. The data bus signals, however, can achieve higher frequency.

Fig. 10 shows the correlation between simulation between simulated and measured noise signal for 'Pattern 1'.

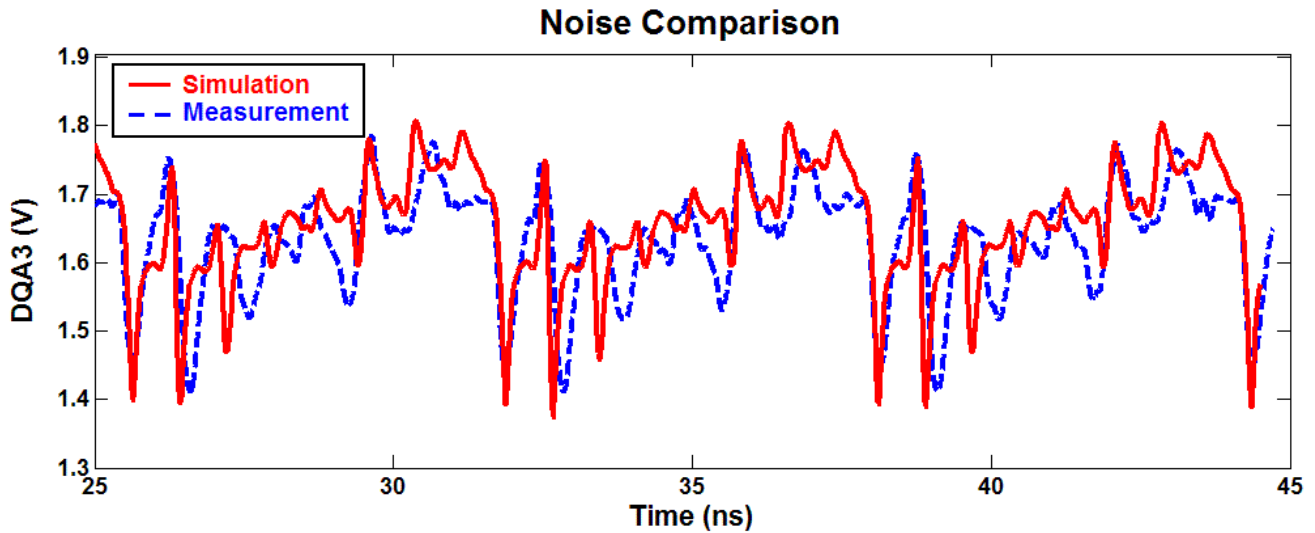


Fig. 10: Correlation of VddIO Supply Noise Simulation and Measurement for 'Pattern 1'

Fig. 11 shows the correlation between measurement and simulation for 'Pattern 2'.

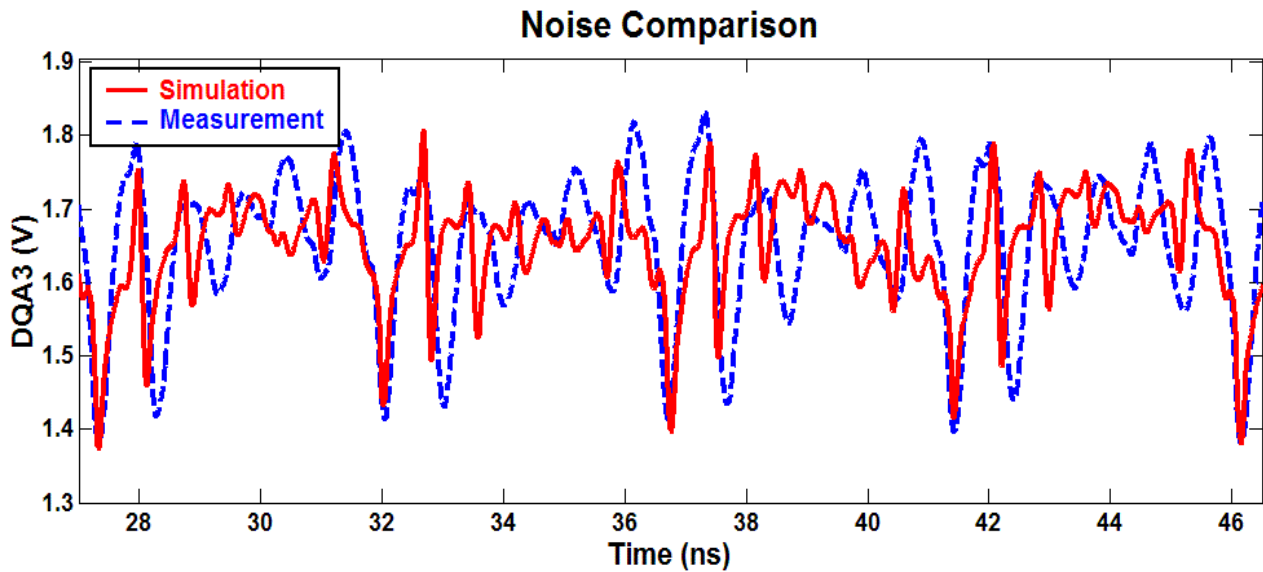


Fig. 11: Correlation of VddIO Supply Noise Simulation and Measurement for 'Pattern 2'

Very good correlation is achieved for both data pattern. The simulated and measured waveforms not only correlate very well in noise amplitude, but they also correlate reasonably well in noise waveform. This confirms the accuracy of the modeling methodology for SSN analysis of interface systems.

The following table summarizes the comparison of simulated and measured supply noise amplitude on the VddIO supply during simultaneous switching of the different pattern:

Pattern Name	Data Signal Pattern	Address/control Signal Pattern	Measured Noise Amplitude	Simulated Noise Amplitude	Amplitude Error
Pattern 1	1100...	1010...	380mV	410mV	8%
Pattern 2	110...	1010...	447mV	431mV	2%

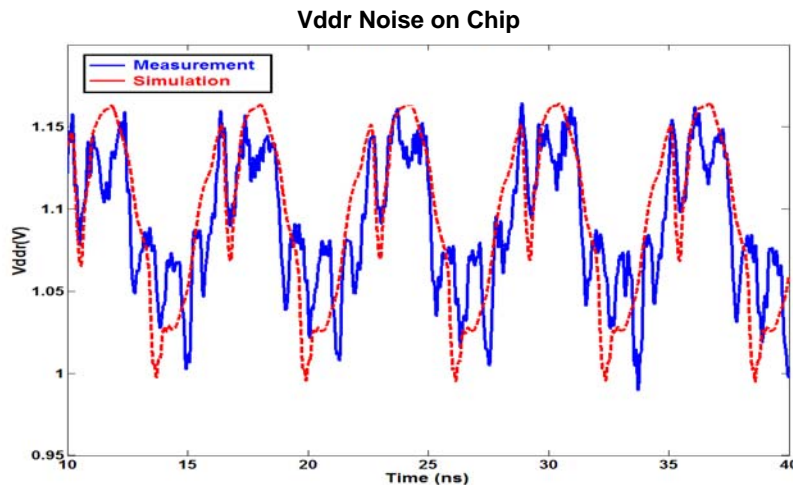
The accuracy of the simulation is noticeably better than 10%.

The table also shows that the noise amplitude for ‘Pattern 2’ is larger than for ‘Pattern 1’. Based on the AC analysis of supply impedances shown in *Fig. 7* the opposite was expected. This demonstrates the limitation of noise predictions based on the AC analysis of supply impedances. Since the AC analysis does not consider the phase offset between different noise contributions, time domain simulations are necessary to predict the accurate noise amplitudes of different excitation patterns.

### V.3. Measuring Supply Noise on Internal Supply Voltage

Measuring supply noise on the internal Vddr rail is more difficult, as there is no direct way to observe this rail from outside the chip. During the chip design, however, differential pairs of large probing pads were added to the top most metal layer to allow measurement of Vddr and ground noise using a differential probe station.

*Fig. 12* shows the correlation of measurement and simulation of Vddr supply noise while the output drivers are transmitting ‘Pattern 1’ listed above.



*Fig. 12:* Correlation of Vddr Supply Noise Simulation and Measurement for ‘Pattern 1’

*Fig. 12* shows a good correlation of the supply noise amplitude for the base frequency component determined by the transmitted data pattern, but the measurement shows more high-frequency noise superimposing this base frequency. The main reason for this discrepancy is that the simulation only includes noise coupled into the Vddr rail

or generated directly by the output drivers. It does not include additional self-induced noise generated by the circuits using V<sub>ddr</sub> as supply. These circuits are operating at a higher frequency and add additional self-induced high-frequency noise to the V<sub>ddr</sub> rail.

The following table summarizes the comparison of simulated and measured supply noise amplitude on the V<sub>ddr</sub> supply during simultaneous switching of the different pattern:

Pattern Name	Data Signal Pattern	Address/control Signal Pattern	Measured Noise Amplitude	Simulated Noise Amplitude	Amplitude Error
Pattern 1	1100...	1010...	179mV	171mV	4%
Pattern 2	110...	1010...	201mV	196mV	2%

Ignoring the high-frequency component not covered by the simulation model, the table shows very good correlation between measured and simulated noise amplitude on V<sub>ddr</sub> for different data pattern. This verifies the modeling strategy for noise coupling in our SSN model.

The dependency of V<sub>ddr</sub> supply noise on the data pattern transmitted by the output drivers is clearly visible. The table also shows that significant noise is generated on this internal supply rail, that can a significant effect on system jitter. Thus, it is mandatory to include this noise analysis into the SSN analysis if the interface system.

#### V.4. Measuring Jitter Sensitivity to Coupled Noise

In order to analyze the impact of signal-to-supply noise on system jitter in the DDR2 interface, the jitter introduced by a single toggling data line was measured and correlated with the supply noise caused by this data line. In this measurement, the data line ‘BA3’ was used to transmit a clock pattern. The jitter on this signal line was measured using an oscilloscope. From the remaining data lines, one data line was transmitting a toggle pattern, creating noise in the system, while the other data lines were kept quite. The jitter caused by this additional noise was measured on the data line ‘BA3’. This measurement was repeated using the remaining data lines one by one as noise generators. *Fig. 13* shows the jitter measured at ‘BA3’ for noise generated at the different signal lines.

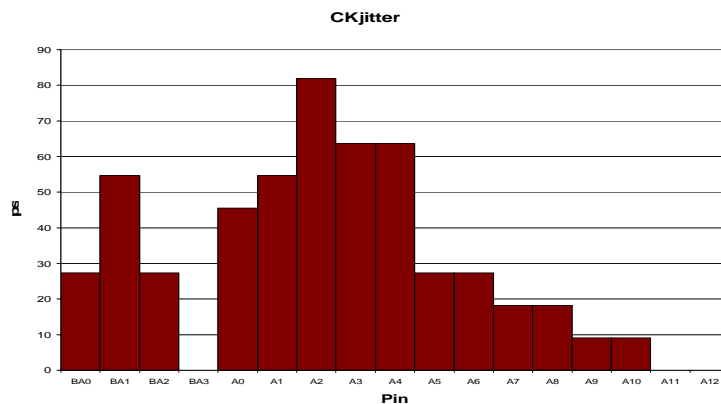
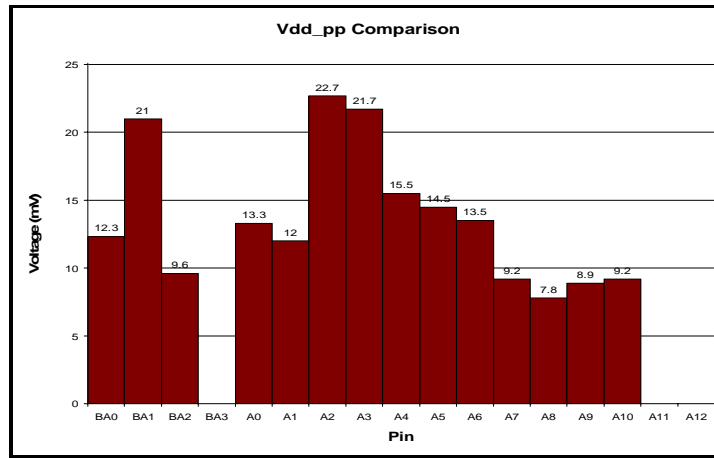


Fig. 13: Jitter caused by Toggle Pattern on Different Signal Lines

The order of signal lines in *Fig. 12* reflects the neighborhood of wire bond pads in the design. It can be seen that the largest jitter is created by signal lines not in the direct vicinity of the signal ‘BA3’ used for jitter measurement. This means, that the observed jitter is not simply caused by signal-to-signal coupling. In this case, we would have expected the jitter to be a clear function of proximity to the signal line ‘BA3’. The pattern in *Fig. 13* cannot be explained by the generation of self-induced noise on the VddIO supply rail either. Since all driver circuits are identical in this measurement, we would expect that each signal creates the same amount of noise on the VddIO rail inside the chip, and therefore, creating the same jitter on the ‘BA3’ line.

We used the SSN analysis model to simulate the supply noise coupled from each signal line into the Vddr supply rail. This noise amount is different for each signal line, as the bonding pattern and the vicinity to supply bonds acting as return paths varies throughout the design. *Fig. 14* shows the supply noise amplitude caused by each signal line when it is toggling. For comparison, the order of signal lines in *Fig. 14* is the same as the order in *Fig. 13*.



*Fig. 14:* Vddr Supply Noise Amplitude Caused by Signal-to-Supply Coupling

The pattern in *Fig. 13* and *Fig. 14* show a close correlation between the noise amplitude on Vddr and the jitter measured at the signal ‘BA3’. This demonstrates that signal-to-supply coupling in a wire-bond package can cause significant amount of noise, and by this add noticeable jitter to the system. The correlation in *Fig. 13* and *Fig. 14* also verifies the accuracy of the noise coupling prediction by the SSN model, despite the use of CCCS based current mirrors for almost all of these signal lines.

## VI. Summary

In this paper we presented the analysis of supply noise for a 667MHz DDR2 system in a low-cost wire-bond package. The high inductance of wire-bond packages poses a serious challenge for power integrity during simultaneous switching events. A detailed understanding and accurate modeling of the worst-case supply noise in such a system is essential to achieve the desired data rate.

We presented a modeling methodology for interface systems that considers not only the supply noise on the output driver supply alone, but also on other supply rails where

noise generated during simultaneous switching events can contribute to system jitter. The supply noise analysis model is compact enough that a large interface with more than 50 lines switching at the same time can be simulated in short time.

Next, a methodology was presented that helps finding activity pattern generating worst-case supply noise in the system. We discussed the limitations of conventional AC supply impedance concepts for interfaces and demonstrated the need for time-domain simulations for supply noise prediction.

Finally, we presented correlations between measurements and simulations of supply noise waveforms and system jitter profiles. These correlations demonstrate the high accuracy of the analysis model. They also confirm the importance of considering noise coupling in these interface systems as a serious source of system jitter.

## VII. References

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