XDR™ Clock Generator

Advance Information

Overview

The XDR™ Clock Generator provides the necessary clock signals to support XDR memory subsystem and Redwood logic interface using a reference clock input with or without spread spectrum modulation. Contained in a 28-pin TSSOP package that includes four differential clock outputs, the XCG provides an off-the-shelf solution for a broad range of high performance interface applications.

Features

- High-speed clock support: 400-800 MHz clock source for XDR memory subsystems and Redwood logic interface
- Quad (open drain) differential output drivers with less than 20 ps short-term jitter
- Spread spectrum reference clock input to minimize EMI
- Differential or single-ended reference clock input: 100 / 133 MHz
- SMBus features: programmable frequency multiplier, select any one to four outputs and mode of operation
- Supports frequency multipliers: 3, 4, 5, 6, 8, 9/2, 15/2 and 15/4.
- Supports systems not requiring synchronization of the XDR clock to another system clock
- Supply Voltage: VDD = 2.5V ± 0.125V

Figure 1 shows the pin assignments of the TSSOP package for the XCG. Table 1 describes the function and connection of each pin.

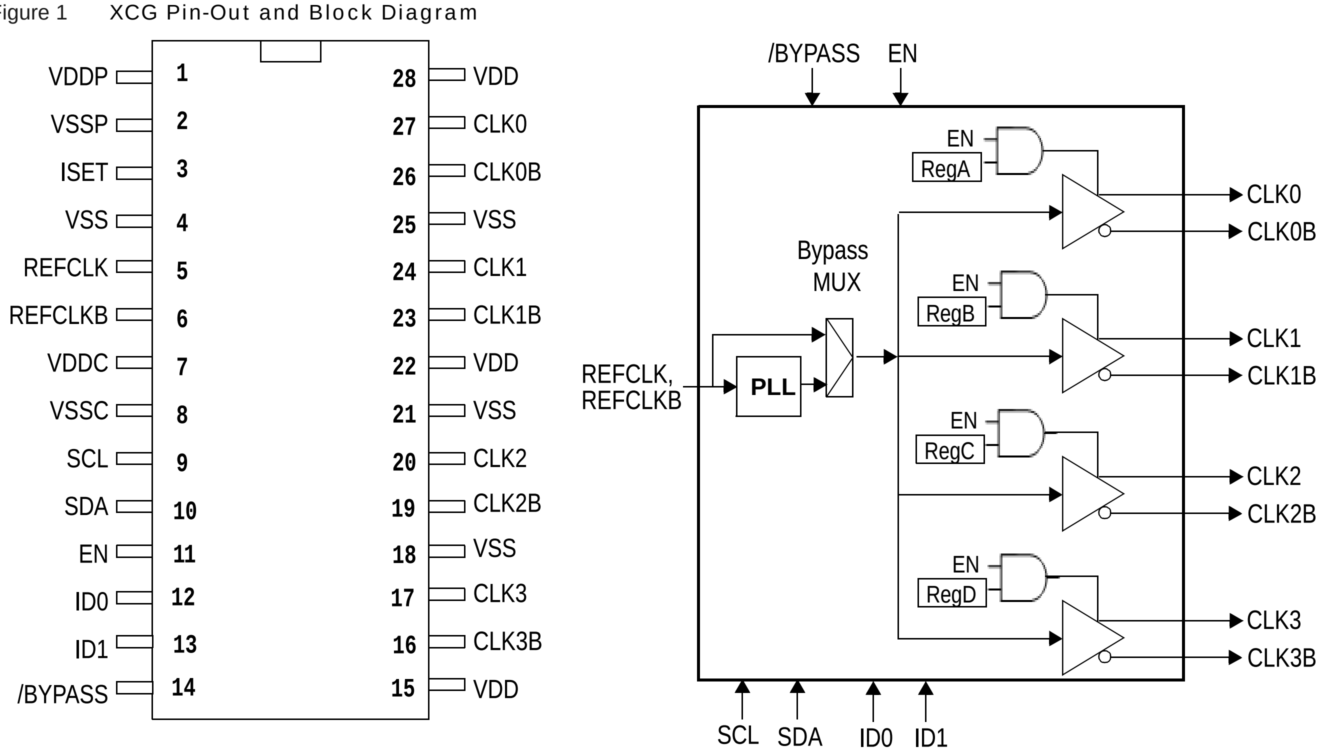
General Description

The block diagram in Figure 1 shows the major components of the XCG. They include a phase lock loop, a bypass multiplexer and four differential output buffers (CLK0/CLK0B, CLK1/CLK1B, CLK2/CLK2B and CLK3/CLK3B). All four outputs can be disabled by a logic low input to the EN pin. An output is enabled when EN is high and a value of 1 is in its SMBus register (RegA-D).

The PLL receives a reference clock input signal, REFCLK, and outputs an intermediate clock signal at a frequency equal to the input frequency times a multiplier. Table 2 shows the multipliers selectable via the SMBus interface. The PLL output clock signal is fed to the differential output buffers to drive the enabled clocks. Disabled outputs are set to high impedance.

The Bypass mode routes the input clock REFCLK to the differential output buffers, bypassing the PLL. Table 3 shows the SMBus control for various modes of operations.

Figure 1 XCG Pin-Out and Block Diagram



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Pin Description

Table 1 **XCG Pin Description**

Pin#	Signal	Type	Function	Notes
1	VDDP	Pwr	Power supply for PLL	2.5V Supply
2	VSSP	G	Ground for PLL	Ground reference
3	ISET	In	Set clock driver current	External resistor
4	VSS	G	Ground	Ground
5	REFCLK	In	Reference clock input	Connect to clock source
6	REFCLKB	In	Complement of reference clock	Connect to clock source
7	VDDC	Pwr	Power supply for core	2.5V supply
8	VSSC	G	Ground for core	Ground reference
9	SCL	In	SMBus Clock	Connect to SMBus
10	SDA	In	SMBus Data	Connect to SMBus
11	EN	In	Output Enable	CMOS signal
12	ID0	In	Device ID	CMOS signal
13	ID1	In	Device ID	CMOS signal
14	/BYPASS	In	REFCLK bypassing PLL	CMOS signal
15	VDD	Pwr	Power supply for clock drivers	2.5V Supply
16	CLK3B	Out	Clock3 output (complement)	Connect to load
17	CLK3	Out	Clock3 output	Connect to load
18	VSS	G	Ground	Ground
19	CLK2B	Out	Clock2 output (complement)	Connect to load
20	CLK2	Out	Clock2 output	Connect to load
21	VSS	G	Ground	Ground
22	VDD	Pwr	Power supply for clock drivers	2.5V Supply
23	CLK1B	Out	Clock1 output (complement)	Connect to load
24	CLK1	Out	Clock1 output	Connect to load
25	VSS	G	Ground	Ground
26	CLK0B	Out	Clock0 output (complement)	Connect to load
27	CLK0	Out	Clock0 output	Connect to load
28	VDD	Pwr	Power supply for clock drivers	2.5V Supply

PLL Multiplier

Table 2 shows the frequency multipliers in the PLL, selectable by programming the SMBus Registers MULT0, MULT1, and MULT2. Default multiplier at power up is 4.

Table 2 **PLL Multiplier Selection**

Register MULT2	Register MULT1	Register MULT0	Frequency Multiplier	Output Frequency (MHz)	
				REFCLK = 100 MHz [a]	REFCLK = 133.3 MHz [a]
0	0	0	3	300 [c]	400
0	0	1	4 [b]	400	533
0	1	0	5	500	667
0	1	1	6	600	800
1	0	0	8	800	- [c]
1	0	1	9/2	450	600
1	1	0	15/2	750	- [c]
1	1	1	15/4	- [c]	500

a. Output frequencies shown in Table 2 are based on nominal input frequencies of 100 MHz and 133.3 MHz. The PLL multipliers are also applicable to spread spectrum modulated input clock at the max and min cycle time shown in Figure 9.
b. Default PLL multiplier at power up.
c. Output at this frequency does not conform to the AC characteristics in Table 12, or output frequency is not supported.

Device ID and SMBus Device Address

The device ID (ID0 and ID1) is a part of the SMBus device 8-bit address. The least-significant bit of the address designates a write or read operation. Table 3 shows the addresses for four XCG devices on the same SMBus.

Table 3 **SMBus Device Addresses for XCG**

XCG		Hex Address	8-bit SMBus Device Address Including Operation							
Device #	Operation		Five Most-Significant Bits					ID1	ID0	WR# / RD
0	Write	D8	1	1	0	1	1	0	0	0
	Read	D9								1
1	Write	DA						0	1	0
	Read	DB								1
2	Write	DC						1	0	0
	Read	DD								1
3	Write	DE						1	1	0
	Read	DF								1

Modes of Operation

The modes of operation are determined by the logic signals applied to the EN and /BYPASS pins, and the values in the five SMBus Registers: RegTest, RegA, RegB, RegC, and RegD. Table 4 shows how to select from one to all four of the outputs, the Outputs Disabled Mode (EN = low) and Bypass Mode (EN=high, /BYPASS=low). There is also an option reserved for vendor test. Disabled outputs are set to Hi-Z.

At power up, the SMBus registers default to the last entry in Table 4. The value at RegTest is 0. The values at RegA, RegB, RegC, and RegD are all 1. Thus, all outputs are controlled by the logic applied to EN and /BYPASS.

Table 4 **Modes of Operation**

EN	/BY PASS	Reg Test	RegA	RegB	RegC	RegD	CLK0/CLK0B	CLK1/CLK1B	CLK2/CLK2B	CLK3/CLK3B
L	X	X	X	X	X	X	Hi-Z	Hi-Z	Hi-Z	Hi-Z
H	X	1	X	X	X	X	Reserved for Vendor Test			
H	L	0	X	X	X	X	[a] REFCLK/ REFCLKB	REFCLK/ REFCLKB	REFCLK/ REFCLKB	REFCLK/ REFCLKB
H	H	0	0	0	0	0	Hi-Z	Hi-Z	Hi-Z	Hi-Z
H	H	0	0	0	0	**1**	Hi-Z	Hi-Z	Hi-Z	**CLK/CLKB**
H	H	0	0	0	**1**	0	Hi-Z	Hi-Z	**CLK/CLKB**	Hi-Z
H	H	0	0	0	**1**	**1**	Hi-Z	Hi-Z	**CLK/CLKB**	**CLK/CLKB**
H	H	0	0	**1**	0	0	Hi-Z	**CLK/CLKB**	Hi-Z	Hi-Z
H	H	0	0	**1**	0	**1**	Hi-Z	**CLK/CLKB**	Hi-Z	**CLK/CLKB**
H	H	0	0	**1**	**1**	0	Hi-Z	**CLK/CLKB**	**CLK/CLKB**	Hi-Z
H	H	0	0	**1**	**1**	**1**	Hi-Z	**CLK/CLKB**	**CLK/CLKB**	**CLK/CLKB**
H	H	0	**1**	0	0	0	**CLK/CLKB**	Hi-Z	Hi-Z	Hi-Z
H	H	0	**1**	0	0	**1**	**CLK/CLKB**	Hi-Z	Hi-Z	**CLK/CLKB**
H	H	0	**1**	0	**1**	0	**CLK/CLKB**	Hi-Z	**CLK/CLKB**	Hi-Z
H	H	0	**1**	0	**1**	**1**	**CLK/CLKB**	Hi-Z	**CLK/CLKB**	**CLK/CLKB**
H	H	0	**1**	**1**	0	0	**CLK/CLKB**	**CLK/CLKB**	Hi-Z	Hi-Z
H	H	0	**1**	**1**	0	**1**	**CLK/CLKB**	**CLK/CLKB**	Hi-Z	**CLK/CLKB**
H	H	0	**1**	**1**	**1**	0	**CLK/CLKB**	**CLK/CLKB**	**CLK/CLKB**	Hi-Z
H	H	**0** [b]	**1** [b]	**1** [b]	**1** [b]	**1** [b]	**CLK/CLKB**	**CLK/CLKB**	**CLK/CLKB**	**CLK/CLKB**

a. Bypass Mode. REFCLK bypasses the PLL to the output drivers.
b. Default mode of operation at power up.

State Transition Latency

Power Up Latency

Table 5 specifies the maximum settling time (t_{PU}) of the CLK0, CLK0B, CLK1, CLK1B, CLK2, CLK2B, CLK3, and CLK3B outputs from device power-up.

Table 5 **State Transition Latency VDD, VDDP and VDDC**

Latency Type	From	To	t_{PU}	Description
Power up	VDD VDDP VDDC on REFCLK & REFCLKB settle	CLK0/ CLK0B, CLK1/ CLK1B, CLK2/ CLK2B, CLK3/ CLK3B Normal	3 ms	Time from VDD, VDDP, and VDDC being applied and settled to clock outputs settled

Change of Operation Latency

Table 6 specifies the maximum settling time (t_{CO})of the CLK0, CLK0B, CLK1, CLK1B, CLK2, CLK2B, CLK3, and CLK3B outputs from the time SMBus programming is completed, or when an output enable (EN) or a bypass (/BYPASS) signal is applied and settled.

There is no latency nor glitches at a clock output if its register receives from the SMBus a new value equal to its current content.

Table 6 **State Transition Latency for SMBus Control, Output Enable and Exiting BYPASS Mode**

Latency Type	From	To	t_{CO}	Description
SMBus or Mode Select Inputs	Last of a complete set of SMBus Programming steps applied to SCL and SDA pins [a] or EN and/or /BYPASS Change State	CLK0/ CLK0B, CLK1/ CLK1B, CLK2/ CLK2B, CLK3/ CLK3B Settled	3 ms	Signals for selecting a mode of operation applied and settled to CLK0/CLK0B CLK1/CLK1B, CLK2/CLK2B, and CLK3/CLK3B outputs settled.

a. There is no output latency nor glitches if an output register receives a new value equal to the current register content from the SMBus.

Power Sequence

The power up sequence of external termination voltage applied to the clock output pins must be equal or slower than the supply voltages of the device.

The power up sequence of input pins SCL, SDA, ID0, ID1, EN and /BYPASS must be equal to or slower than the supply voltages of the device.

Device Parameters

This section specifies the numerical values of the physical parameters described earlier in this document.

The XDR clock source meets the device characteristics listed in Table 10 and Table 12 when characterized under the operating conditions listed in Table 9 and Table 11, and when using the components shown in Figure 3, and the corresponding component values given in Table 13 and its footnote.

Only the DC specifications of Table 10 apply while in Bypass mode. The AC specifications of Table 12 do not apply while in Bypass mode unless specified otherwise.

Absolute Maximums

Table 7 represents stress ratings only, and functional operation at the maximum settings is not guaranteed.

Table 7 **Absolute Maximum Ratings**

Symbol	Parameter	Min	Max	Unit
$V_{DD,ABS}$	Max voltage on V_{DD} with respect to ground	-0.3	2.8	V
$V_{I,ABS}$	Max voltage on any pin with respect to ground	-0.3	V_{DD}+ 0.25	V

Supply Current Characteristics

The current drawn through the V_{DD} pins is specified in Table 8. This includes the total current through all $V_{DD,}$ V_{DDP} and V_{DDC} pins.

Table 8 **Supply Current Characteristics**

Symbol	Parameter	Min	Max	Unit
I_{NORMAL}	Current in Normal state		TBD	mA

DC Operating Conditions

This section specifies input conditions for operating the device. When operated outside these limits, device characteristics are undefined.

Table 9 **DC Operating Conditions**

Symbol	Parameter	Min	Max	Unit
V_{DDP}	Supply voltage for PLL	2.375	2.625	V
V_{DDC}	Supply voltage for core	2.375	2.625	V
V_{DD}	Supply voltage for clock buffers	2.375	2.625	V
$V_{IH,CLK}$	Input high voltage for differential clock REFCLK/REFCLKB	0.6	0.95	V
$V_{IL,CLK}$	Input low voltage for differential clock REFCLK/REFCLKB	-0.15	+0.15	V
$V_{IX,CLK}$	REFCLK/REFCLKB crossing point voltage	200	550	mV
$\Delta V_{IX,CLK}$	Difference in REFCLK/REFCLKB crossing point voltages	-	150	mV
V_{TH}	Input threshold voltage for single-ended REFCLK [a]	0.35	$0.5V_{DD}$	V
$V_{IH,SE}$	Input signal high voltage for single-ended REFCLK	V_{TH} + 0.3	2.625	V
$V_{IL,SE}$	Input signal low voltage for single-ended REFCLK	-0.15	V_{TH} - 0.3	V
V_{IH}	Input signal high voltage at ID0, ID1, EN and /BYPASS	1.4	2.625	V
V_{IL}	Input signal low voltage at ID0, ID1, EN and /BYPASS	-0.15	0.8	V
$V_{IH,SM}$	Input signal high voltage at SCL and SDA [b]	1.4	3.465 [b]	V
$V_{IL,SM}$	Input signal low voltage at SCL and SDA	-0.15	0.8	V
T_A	Ambient operating temperature	0	70	°C

a. When using single-ended clock input, V_{TH} is supplied to the REFCLKB pin as shown in Figure 2. Duty-cycle of single-ended REFCLK input is measured at V_{TH}.

b. This range of SCL and SDA input high voltage allows the XCG to co-exist with 3.3V, 2.5V and 1.8V devices on the same SMBus.

DC Characteristics

This section specifies the device characteristics when using the external circuits as shown in Figure 3 with component values listed in Table 13 and its footnotes.

Table 10 **DC Device Characteristics**

Symbol	Parameter	Min	Nominal	Max	Unit
V_{OX}	Differential output crossing-point voltage [a]	0.9	1.0	1.1	V
V_{COS}	Output voltage swing (peak-to-peak single-ended) [b]	300	325	350	mV
$V_{OL,ABS}$	Absolute output low voltage at CLK0, CLK0B, CLK1, CLK1B, CLK2, CLK2B, CLK3 and CLK3B pins [c]	0.85	-	-	V
V_{ISET}	Reference voltage for swing control current, I_{ref}, across max and min V_{DD} and operating temperatures. (I_{ref} is the current flowing through the swing control resistor R_{RC} installed between the ISET pin and ground as shown in Fig. 3. [d])	0.98	1.0	1.02	V
I_{OL}/I_{ref}	Ratio of output low current to reference current at nominal V_{DD}	6.8	7.0	7.2	-
$I_{OL,ABS}$	Minimum Current at $V_{OL,ABS}$ [e]	45	-	-	mA
$V_{OL,SDA}$	SDA output low voltage at test condition of SDA output low current equal to 4mA	-	-	0.4	V
$I_{OL,SDA}$	SDA output low current at test condition of SDA output low voltage equal to 0.8V	6	-	-	mA
I_{OZ}	Current during Hi-Z per pin at CLK0, CLK0B, CLK1, CLK1B, CLK2, CLK2B, CLK3 and CLK3B	-	-	50	µA

a. V_{OX} is measured on external divider as shown in Figure 3.
b. V_{COS} = (clock output high voltage — clock output low voltage), at the measurement points shown in Figure 3, excluding overshoot and undershoot.
c. $V_{OL,ABS}$ is measured at the clock output pins of the package, instead of the measurement points in Figure 3.
d. I_{ref} is equal to V_{ISET} / R_{RC}. Tolerance of R_{RC} needs to be +/-1% or smaller.
e. Minimum $I_{OL,ABS}$ is measured at the clock output pins of the package with the termination resistors in Figure 3 being R_1 = 34Ω, R_2 = 31.8Ω, R_3 = 48.7Ω, R_T = 28Ω and R_{RC} = 147Ω, V_{TS} = 2.5V and V_T = 1.2V

AC Operating Conditions

This section specifies input AC conditions for operating the device. When operated outside these limits, device characteristics are undefined.

Table 11 **AC Operating Conditions**

Symbol	Parameter	Min	Max	Unit
$t_{CYCLE,IN}$	REFCLK/REFCLKB input cycle time	7	11	ns
$t_{J,IN}$	Input cycle-to-cycle jitter [a]	-	185	ps
DC_{IN} [b]	Input duty-cycle over 10,000 cycles	40%	60%	t_{CYCLE}
$t_{CR,IN}$, $t_{CF,IN}$	Rise and fall time (measured at 20% - 80% of input voltage) for REFCLK/REFCLKB inputs	175	700	ps
$t_{CR,CF,IN}$	Difference between input rise and fall times on the same pin of a single device (20% - 80%)	-	150	ps
$f_{M,IN}$ [c]	Input frequency of modulation	30	33	kHz
$P_{M,IN}$ [c]	Modulation index for triangular modulation	-	0.6	%
	Modulation index for non-triangular modulation	-	0.5[d]	%
$t_{SR,IN}$	Input slew rate (measured at 20% - 80% of input voltage) for REFCLK	1	4	V/ns
$C_{IN,PD}$	Input capacitance at REFCLK[e]	-	7	pF
$C_{IN,CMOS}$	Input capacitance at scalable CMOS pins (excluding REFCLK)[f]	-	10	pF
$t_{CYCLE,TEST}$	REFCLK Input cycle time in Bypass Test mode	4	40	ns
f_{SCL}	SMBus clock frequency input at SCL pin	10	100	kHz

a. RefClk jitter measured at (V_{IH} (nom) –V_{IL}(nom)) / 2 and is the absolute value of the worst-case deviation.
b. Measured at crossing points for differential clock input or at input threshold voltage V_{TH} for single-ended clock input.
c. If input modulation is used; input modulation is allowed but not required.
d. The amount of allowed spreading for any non-triangular modulation is determined by the induced downstream tracking skew, which cannot exceed the skew generated by the specified 0.6% triangular modulation. Typically, the amount of allowed non-triangular modulation is about 0.5%.
e. Capacitance measured at Frequency = 1MHz, DC bias = 0.9V, and VAC < 100mV.

AC Characteristics

Table 12 gives the AC characteristics for device operation using the external circuits as shown in Figure 3 with component values listed in Table 13 and its footnote.

Table 12 **AC Device Characteristics**

Symbol	Parameter	Min	Max	Unit
t_{CYCLE}	Clock cycle time [a]	1.25	2.5	ns
t_J	Jitter over 1–6 clock cycles at 400–635 MHz [b]	-	40	ps
	Jitter over 1–6 clock cycles at 636–800 MHz [b]	-	30	ps
Δt_{skew}	Drift in t_{skew} when operating temperature varies between 0^oC and 70^oC, and supply voltage between 2.375V and 2.625V [c] .	-	15	ps
DC	Long-term average output duty-cycle	45%	55%	t_{CYCLE}
$t_{DC,ERR}$	Cycle-to-cycle duty-cycle error at 400–635 MHz	-	40	ps
	Cycle-to-cycle duty-cycle error at 636–800 MHz		30	ps
t_{CR} , t_{CF}	Output rise and fall times at 400–800 MHz (measured at 20%–80% of output voltage)	100	300	ps
$t_{CR,CF}$	Difference between output rise and fall times on the same pin of a single device (20%–80%) at 400–635 MHz	-	100	ps
Z_{OUT}	Output dynamic impedance when clock output signal is at V_{OL} = 0.9V [d]	750	-	W

a. Max. and min. output clock cycle times are based on nominal output frequency of 400 and 800 MHz, respectively. For spread spectrum modulated differential or single-ended REFCLK, the output clock tracks the modulation of the input.

b. Output short-term jitter spec is the absolute value of the worst-case deviation and is defined in the Jitter section.

c. t_{skew} is the timing difference between any two of the four differential clocks and is measured at common mode voltage. Δt_{skew} is the change in t_{skew} when the operating temperature and supply voltage change.

d. Zout is defined at the output pins.

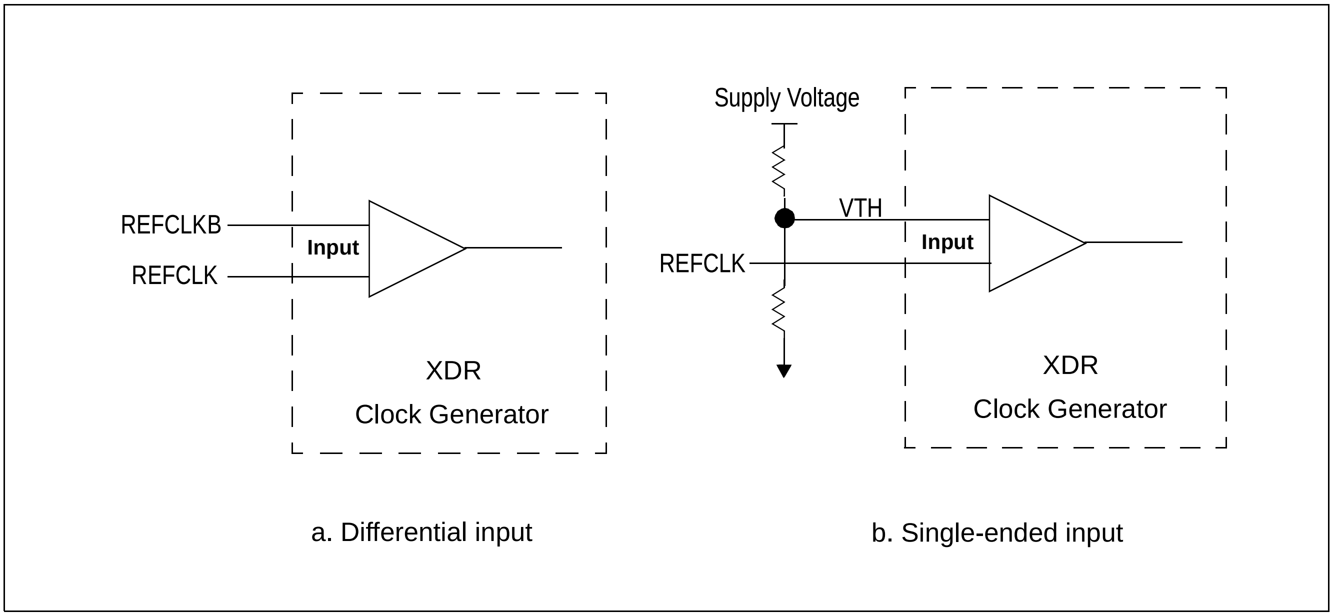
Input Clock Signal

The XCG receives either a differential (REFCLK/REFCLKB) or a single-ended reference clock input (REFCLK).

When the reference input clock is from a differential clock source, it must meet the voltage levels and timing requirements listed in Table 9 and Table 11.

For a single-ended clock input, an external voltage divider and a supply voltage as shown in Figure 2, provide a reference voltage V_{TH} at the REFCLKB pin to determine the proper trip-point of REFLCK. For the range of V_{TH} specified in Table 9, the outputs also meet the DC and AC characteristics in Table 10 and Table 12.

Figure 2 Differential and Single-Ended Reference Clock Inputs



Clock Output Driver

Figure 3 Example System Clock Driver Equivalent Circuit

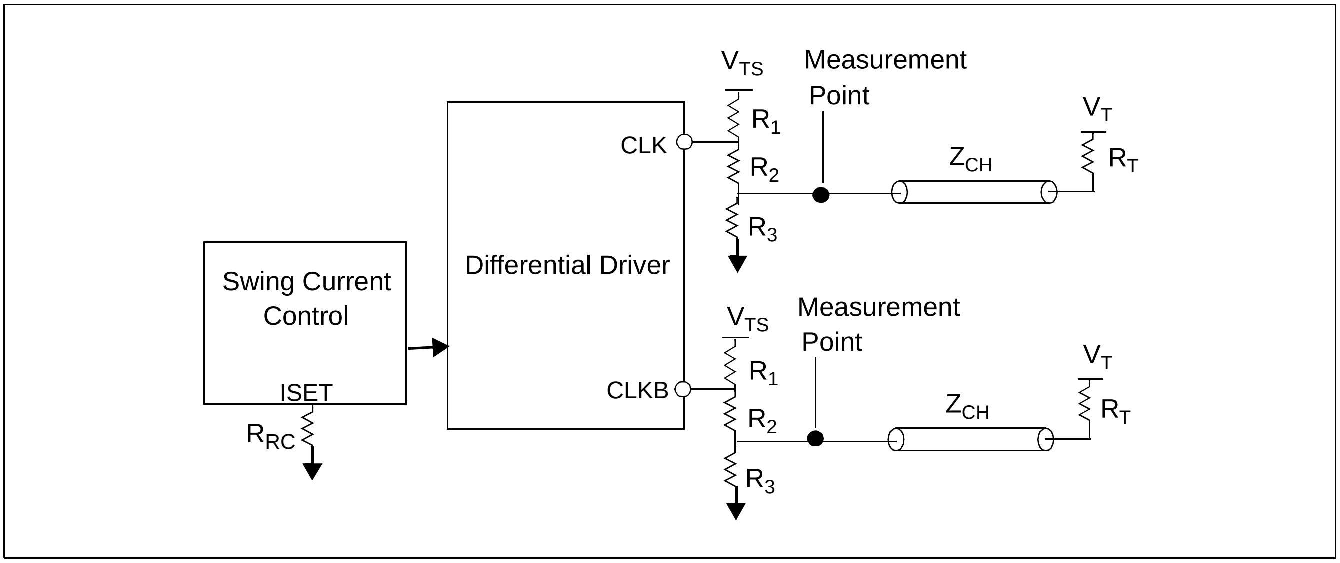


Figure 3 shows the clock driver equivalent circuit. The differential driver produces a specified voltage swing on the channel by switching the currents going into CLK and CLKB. The maximum current is set by an external resistor R_{RC} at the ISET pin, and the minimum is zero. The sum of the CLK and CLKB currents is constant.

The voltage at the ISET pin, V_{ISET}, is, by design, equal to 1V nominally, and the driver current seven times the current flowing through R_{RC}. Hence, the output low driver current can be estimated by $I_{OL} = 7 / R_{RC}$.

The driver output characteristics are defined together with the external resistors R_1 , R_2 , and R_3. The output clock signals are specified at the measurement points indicated in Figure 3. Table 13 shows example values for the resistors.

R_1 , R_2 , R_3 , and the impedance of the clock driver, z_{OUT} , must match the impedance of the channel, z_{CH} , in order to minimize secondary reflections. To accomplish this, z_{OUT} is designed to be 1000 Ω minimum. The effective impedance can be estimated by:

$(1000R_1/(1000 + R_1)+R_2)R_3/(1000R_1/(1000 + R_1)+R_2+R_3)$

Pull-up resistor R_T terminates the transmission line on the other end to minimize reflections of the clock signal.

Table 13 shows the resistor values for establishing an effective source termination impedance of 49.2 Ω to match a 50 Ω channel. The termination voltages are 2.5V for V_{TS} and 1.2V for V_T.

The resister values R_1 = 38.3 Ω, R_2 = 19.1 Ω, R_3 = 54.9 Ω and R_{RC} = 200 Ω can be used to match a 28 Ω channel.

Table 13 **Example External Resistor Values and Termination Voltages for a 50 W Channel** [a]

Symbol	Parameter	Value	Tolerance	Unit
R_1	Termination resistor	39.2	± 1%	Ω
R_2	Termination resistor	66.5	± 1%	Ω
R_3	Termination resistor	93.1	± 1%	Ω
R_T	Termination resistor	49.9	± 1%	Ω
R_{RC}	Swing Control resistor	200	± 1%	Ω
V_{TS}	Source termination voltage	2.5V	± 5%	V
V_T	Termination voltage	1.2V	± 5%	V

a. A different set of resistors (R_1 = 34 Ω, R_2 = 31.8 Ω, R_3 = 48.7 Ω, R_T = 28 Ω ,R_{RC} = 147 Ω) V_{TS} = 2.5V and V_T = 1.2V are used in Figure 3 when testing the minimum of $I_{OL,ABS}$, stated in Table 10.

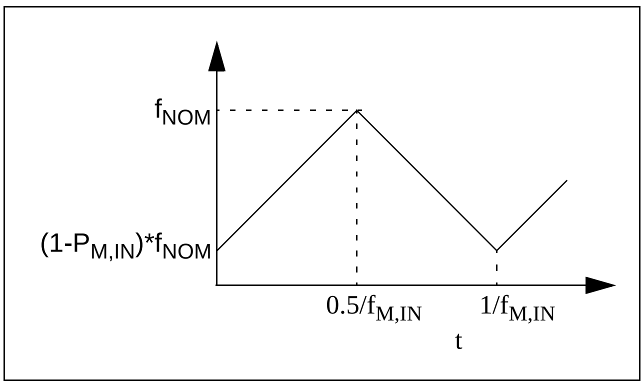
Spread Spectrum Clocking

Spread Spectrum Clocking (SSC) can be used to reduce the spectral peaks and help reduce system-level EMI. The XCG does not contain any functionality to generate SSC. If SSC is used, and the SSC clock input meets the operating conditions listed in Figure 4, the input clock will be modulated and the XCG will track the input modulation. The use of SSC is optional and the input clocks may or may not be modulated.

The minimum clock period cannot be violated. The preferred method is to adjust the spreading to not allow for modulation above the nominal frequency. This technique is often referred to as “downspreading.” An example frequency modulation is shown in Figure 4. The frequency is spread from f_{NOM} down to (1-PM,IN)*f_{NOM}, where f_{NOM} is the inverse of the nominal input cycle time, $t_{CYCLE,IN}$.

The example in Figure 4 shows triangular frequency modulation. Other types of non-linear modulation are commonly used. The amount of allowed modulation index depends on the type of modulation used. Generally, the amount of non-linear modulation allowed is less than the amount of linear (triangular) modulation allowed. The amount of allowed spreading for any non-triangular modulation is determined by the induced downstream PLL tracking skew, which cannot exceed the amount of skew generated by a triangular modulation of the specified amount.

Figure 4 Input Frequency Modulation



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