

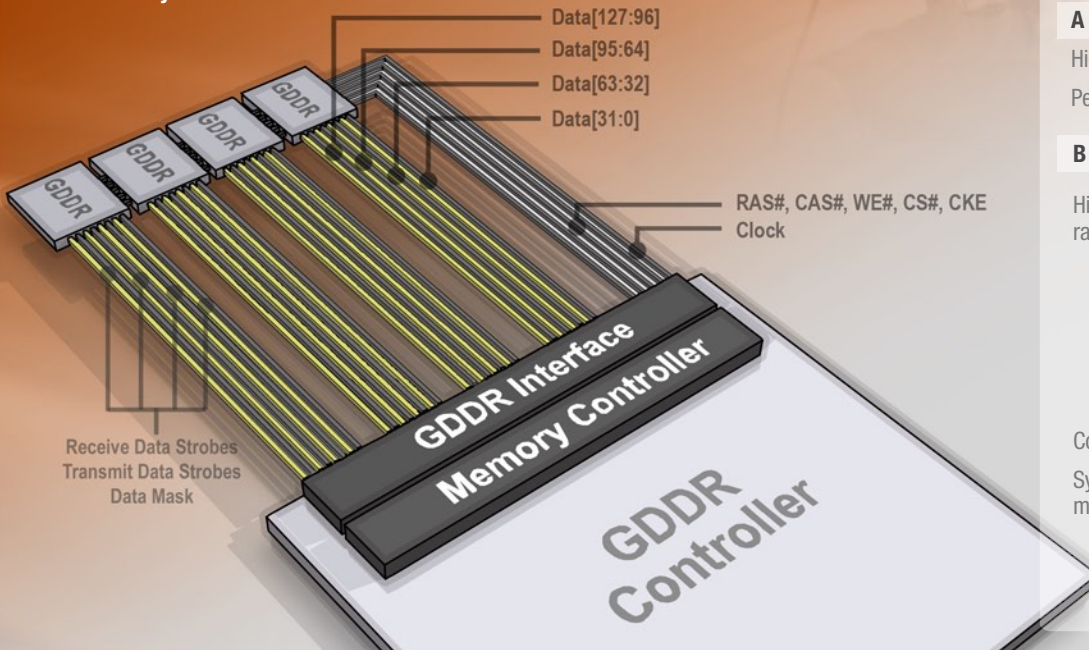
Rambus®

GDDR

Memory Controller Interface Brief



GDDR3 System



APPLICATIONS

High-performance graphics processors
Performance consumer devices

BENEFITS

Highly flexible controller interfaces supporting a wide range of memory types and performance levels

Performance graphics memory (GDDR1/GDDR2/GDDR3)

Main memory (DDR1/DDR2)

Optional support for high performance XDR memory

Complete drop-in macro-cells

System engineering services for reduced time-to-market

Performance Graphics Memory Interface Solution

Rambus GDDR Interface Cells and Services Bring Performance to Graphics Designs

Graphics and multimedia applications require high memory bandwidth to render life-like 3D images and buffer the large amount of frame data for image and video processing. In these applications, higher memory bandwidth translates directly into higher system performance, faster frame rates, and more features.

Graphics and multimedia logic chips need memory interfaces that deliver high bandwidth from a small number of components. These interfaces must often support not only high-speed specialty graphics DDR such as GDDR1/2/3, but also high-speed variants of main memory (DDR2). With current data rates of GDDR components exceeding 1GHz, memory interfaces for graphics and multimedia are challenging to design.

Rambus GDDR interface cells and services provide a comprehensive solution for high-bandwidth performance memory systems. With an emphasis on promoting customer success, Rambus DDR solutions include a family of interface cells, system and package design services, and bring-up support. Furthermore,

Rambus GDDR solutions offer optional modes to higher performance levels.

Complete Drop-In Cells Using Proven Circuit Technology

Rambus GDDR interface cells are complete, integrated macro-cells, incorporating all required components such as the IO pads, delay-locked loop, clock and power distribution, and control logic.

These fully-assembled interface cells integrate seamlessly into customers' logic chips, and are optimized for high performance from a small number of memory components. As with other Rambus memory interface cells, this approach improves time-to-market, lowers design risk, and enables high-frequency operation.

System Engineering Services for Reduced Time-to-Market

In addition to memory interface cells, Rambus offers system engineering services as part of the complete interface solution. At 1 GHz and beyond, system-level considerations such as package signal mapping and system board routing are essential to signal integrity on GDDR memory systems. Rambus provides

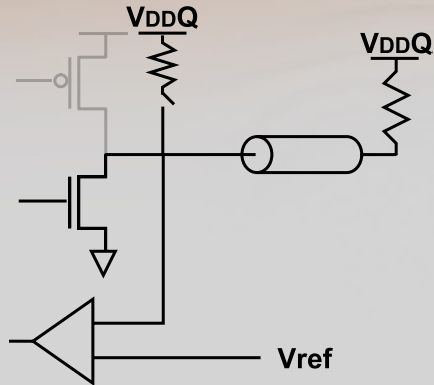
engineering services such as package design, system board layout, reference guidelines, and bring-up assistance to ensure our interface works in the application environment. These system engineering services also improve time-to-market and support robust system operation in mass production. With over a decade of experience in high-speed system design, Rambus is a leader in providing total system solutions for performance memory systems.

Optional Modes to Higher Performance

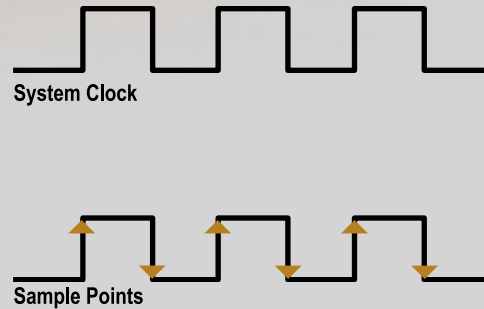
Since many graphics and multimedia applications benefit from the highest attainable memory performance, Rambus offers GDDR interfaces with an optional performance mode to XDR DRAM, enabling higher memory bandwidths. This capability allows customers to develop a single chip that can reach higher performance levels, while continuing to service lower price-performance points.

1.6GHZ BI-DIRECTIONAL SIGNAING
(1.8V PSEUDO-OPEN DRAIN LOGIC)

DOUBLE DATA RATE (DDR)



GDDR3 Physical Signaling System



FEATURES

Low-latency performance graphics memory interface

High-speed GDDR1/GDDR2/GDDR3/DDR2 signaling modes

- 400 MHz to 1.6 GHz data rates
- SSTL_18 and 1.8 V pseudo open-drain logic levels
- Double data rate signaling

Variable data bit-widths

- Available in 32-bit, 64-bit interfaces with optional ECC support

Complete drop-in macro-cell using proven circuit technology

- Fully-integrated cell includes IO pads, delay-locked loop (DLL), on-die termination, global clock distribution, and power routing

GDDR Interface Cell

The Rambus GDDR interface cell is a hard macro providing the physical layer between the controller logic and GDDR components. The interface cell contains the calibrated IOs pads for 400 MHz to 1.6 GHz data rates, low-jitter delay-locked loop, calibrated on-die termination, and data resynchronization circuitry.

GDDR Signaling

The interface cell is programmable to both series-stub-terminated and pseudo open-drain logic levels, allowing compatibility with GDDR1/GDDR2/ GDDR3 and DDR2 memory components. The interface cell supports both SSTL_1.8 and 1.8V pseudo open-drain logic levels.

Design and Integration Support

Rambus GDDR cells come with a complete set of design models and integration tools, including GDSII database, timing models, layout verification netlists, gate-level models, place-and-route outline, and placement guidelines. These models and tools reduce the integration effort and lower engineering costs.

Flexible, Highly-Configurable Solution

Rambus GDDR interfaces are available in varying bit widths, from 32-bit to 256-bit, with optional error correction code (ECC) support. The circuit architecture is designed to support a wide variety of CMOS microfabrication processes such as 65 nm, 90 nm, 0.13 μm , and 0.18 μm .

Interface Features

- Calibrated output impedance
- Programmable on-die termination (60-240 Ω)
- Integrated delay locked loop (DLL)

- FlexPhase™ timing adjustment of data, address, and clock signals
- Synchronous ASIC interface for compatibility with synthesizable design flows
- Programmable output slew rate
- Differential bi-directional, single-ended bi-directional data strobe, and single-ended unidirectional data strobe support
- Input receiver and output transmitter enable control
- Optional ECC support

Testability Features

- ATPG Scan (parallel interface scan test)
- IO Wrap Loopback Test
- IDDQ mode
- BIST (built-in self test)
- Optional FlexPhase™ system timing margin measurement

Interface Cells and Models

- GDSII database
- Layout verification netlists (CDL)
- Behavioral and gate-level models
- Place-and-route outline
- ASIC interface timing model

System Engineering Services

- Package ball-out mapping and signal assignment
- Package escape routing guidelines
- System board design
- Power delivery guidelines
- System clocking strategy
- Reference design consulting

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