

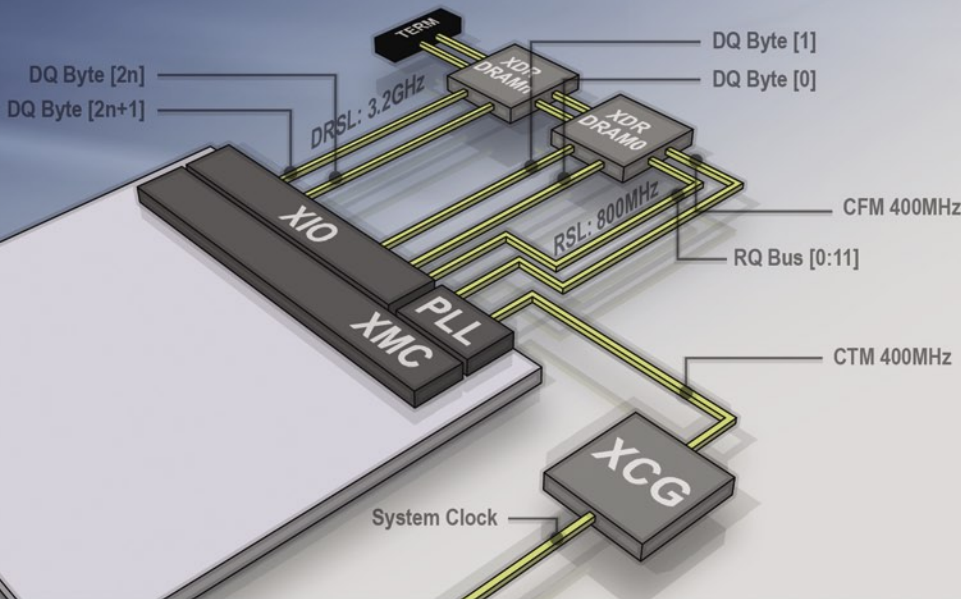
Rambus®

XDR™

DRAM Product Brief



XDR DRAM System Example



APPLICATIONS

- Consumer Electronics
- Computer Graphics
- Server Main Memory
- Networking
- Supercomputing

BENEFITS

- Highest bandwidth for demanding applications
- Fast time-to-market
- Simplified system design and test with FlexPhase™
- Minimized risk from fully validated designs
- Scalable with Dynamic Point-to-Point technology
- System engineering services for reduced time-to-market
- XDIMM module support for high capacity applications

High Performance Memory Interface Solution

XDR DRAM: Delivers a Quantum Leap in Memory Bandwidth

The Rambus XDR DRAM achieves an order of magnitude increase in DRAM bandwidth over today's best-of-class memory systems. The XDR DRAM interface uses a small number of very high-speed signals to carry all address, data, and control information.

XDR DRAM provides a total system solution to many of the complex issues and problems that engineers face in designing cost effective, high-performance memory subsystems. A single, 2-byte wide, 3.2 GHz XDR DRAM component provides up to 6.4 GB/sec bandwidth. The XDR solution was engineered to be effective in small footprint, high-bandwidth consumer systems as well as in high-performance main memory applications. The XDR roadmap supports a performance path up to 8GHz data rates delivering up to 16 Gigabytes / second per DRAM.

A Solution for High Bandwidth Applications

Computer processors continue to place higher demands on the DRAM memory subsystem. XDR DRAM will deliver on the increasing front-side-bus performance requirements. XDR memory is ready to deliver the highest

bandwidths necessary to meet the demands of these CPUs.

Consumer products such as game consoles and digital TV chipsets that demand high-performance memory bandwidth are able to use 6.4 to 16 GB/sec bandwidth available from a single x16 XDR DRAM component.

DTV chipsets are consolidating increasing numbers of high-definition MPEG2 image decode streams with new advanced features such as hard-disk recording, video conferencing and broadband gateways.

Next generation desktop GPUs require increasing memory bandwidth for realistic real-time rendering of graphics and video sequences. These end-user experiences translate to upwards of 50 GB/sec and beyond from a 64 to 128-bit data buses to supply the needed memory bandwidth.

XDR DRAM delivers the complete system solution for these new generation CPUs with memory bandwidth intensive applications.

XDR DRAM: The Bandwidth Leader

The XDR memory is a CMOS DRAM available in varying bit capacities; it has a native data bus width of 16 bits. Devices can be

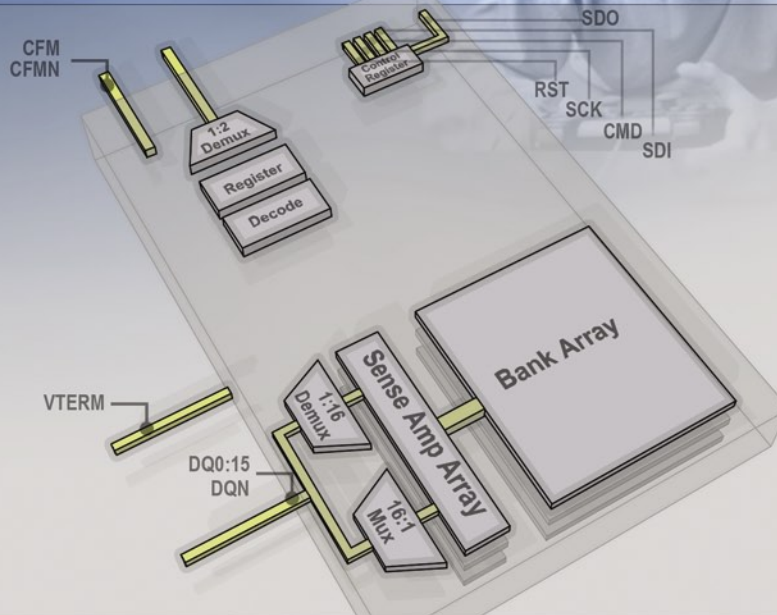
independently programmed to be 1, 2, 4, or 8 bits wide to support Dynamic Point-to-Point topologies. The XDR DRAM data bus uses DRSL technology and octal data rate transfers. A typical x16 XDR DRAM device can sustain data bandwidths ranging from 6.4 to 16 GB/sec.

The XDR architecture allows high sustained bandwidth for multiple, interleaved, randomly addressed memory transactions. The device's eight bank architecture supports multiple interleaved transactions for maximum performance.

XDR DRAM Interface Signaling

XDR signaling solutions use the best of both worlds, Differential Rambus Signaling Levels (DRSL) for scalable high speed point to point bi-directional data signals and Rambus Signaling Levels (RSL) for source synchronous bussed address and command signals to multiple DRAM devices. The point to point bus allows multi-GHz speeds, while the bussed address allows scalable capacity of up to 36 DRAM devices per request bus block.

XDR DRAM Block Diagram



FEATURES

Highest pin bandwidth

- 3.2 to 8.0 GHz data rate
- Octal Data Rate (ODR) signaling
- Bi-directional differential RSL (DRSL)
- Programmable on-chip termination
- Adaptive impedance matching
- Dynamic Point-to-Point scalability

Highest sustained device bandwidth

- 6.4 to 16 GB/sec sustained data rate
- Bank-interleaved transactions at full bandwidth
- Early-read-after-write support for maximum efficiency
- Zero overhead refresh

Low power

- 1.8V Vdd
- Programmable ultra-low-voltage I/O signaling
- Power-down self-refresh support
- Dynamic data width support
- Per pin I/O power-down

The combination of DRSL and RSL signaling provides a high-performance interconnect for the most demanding of applications. Ultra-low-voltage-swing-differential signals minimize di/dt, thereby:

- Reducing ground bounce
- Decreasing power consumption
- Reducing electromagnetic interference
- Increasing scalability to higher data rates
- Improved noise immunity via common mode rejection

Octal Data Rate Transfers

Octal Data Rate transfers are used between the XDR ASIC controller and the XDR DRAM. Eight bits of data per clock are transferred per 400MHz clock cycle effectively delivering data at 3.2GHz data rates. The XDR DRAM data rates are scalable to 8.0 GHz as bandwidth needs increase.

Manufacturability

The XDR DRAM is a memory component manufactured by Rambus's memory partners. The DRAM contains a compliant XDR DRAM interface specified by Rambus and a standard DRAM memory core. Compliant XDR DRAM components can vary in memory density, page size, core speed grade, and data bus width.

Each vendor's XDR device is described by their individual vendor component datasheets. However, the XDR architecture ensures interoperability between components of similar architecture from different memory vendors.

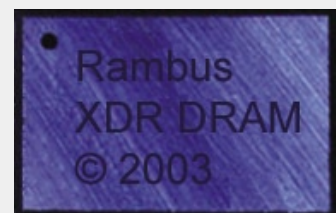
Bandwidth and Lower System Cost

XDR DRAM furnishes not only high-bandwidth memory performance but also enables low cost systems. XDR DRAM is compatible with mainstream cost-effective four-layer PCB designs. DRSL and ultra-low-voltage-swing signaling helps to minimize the effects of EMR, di/dt, and power. XDR DRAM's highest-per-component bandwidth helps to minimize DRAM component count without sacrificing performance or minimum memory granularity. Memory modules using XDR components maximize performance per module while supporting industry standard form factors and densities — without sacrificing memory bandwidth or latency.

Solutions for System Problems

The XDR memory architecture was designed as a complete system solution. This product family solves the many problems facing design engineers developing high-volume, cost-effective, and high-performance memory subsystems.

XDR DRAM CSP PACKAGE



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