On-chip Power Supply Noise Monitor

Designed to give SoC designers a better understanding of the effects of power supply noise on circuit performance, and ultimately, improve the chip quality and reduce time-to-market.

Overview

Our On-chip Power Supply Noise Monitor is a compact IP block embedded directly into the SoC that accurately measures power supply noise in low-power, high-performance interfaces and electronic systems.

It was developed to overcome the characterization challenges of low-power, high-performance interfaces and electronic systems. The Noise Monitor is embedded on-chip and works in conjunction with our LabStation™ Validation Platform to enable noise measurements directly on the chip, eliminating the need for hand probing.

The Noise Monitor accurately captures high-frequency noise components in both the time and frequency domain. It also includes a Noise Generator that can be used in conjunction with noise and jitter measurements to extract power distribution network impedance (ZPDN) and power supply noise induced jitter (PSIJ) sensitivity.

Noise Monitor Implementation Example

![Noise Monitor Implementation Example Diagram]

Highlights

- Low area overhead IP block embedded on chip for localized noise measurements
- Measures cyclostationary power supply noise in both time and frequency domain
- Extracts power distribution network impedance
- Can be used with jitter measurements to derive power supply noise induced jitter (PSIJ)
- Measurement bandwidth extends up to 6GHz
- JTAG-compatible macro for easy integration
- Includes easy-to-use LabStation™ software for automated measurements, post-processing, and data visualization

Applications

- In-situ, on-chip characterization of power-supply noise in complex SoCs
- Validation of SoC on-chip bypassing and package design
- Characterization of timing jitter sensitivity in critical circuits
- Validation of power distribution networks (PDNs) in electronic systems
- Debug and validation of power integrity in high-performance electronic systems
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Noise Monitor Configuration

Features
- Available for TSMC40G/LP, GF28HPP/SLP, and Samsung 28LPP fabrication processes
- IJTAG-compatible for easy integration
- Voltage support for thin- and medium-oxide thickness devices
- Universal layout compatible with North-South and East-West orientations
- Voltage resolution: 200µV/LSB
- Frequency resolution: 1MHz
- Effective Measurement BW: Up to 3-6GHz
- LabStation software for automated measurements, post-processing and data visualization

Example Results

Deliverables
- Fully-characterized hard macro
- Complete design views:
  - Behavioral model
  - Verification test benches
  - Layout abstracts (.lef)
  - Timing models (.lib)
  - Verilog models
  - ATPG models
  - GDSII layout
- Full documentation:
  - Integration guide
  - ASIC/DFT manufacturing guidelines
  - CDL netlists (.cdl)
  - DRC & LVS reports
  - Noise Monitor user guide
- Software:
  - LabStation software

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