Rambus

MEMORY + INTERFACES
R+ DDRn PHYs
Product Brief

R+LPDDR3 DRAM

Improved power consumption and performance in smartphones and tablets, while maintaining compatibility with standard LPDDR3.

Overview

The R+™ LPDDR3 DRAM brings next-generation, low-power DRAM performance to the market today. The Rambus enhanced R+ LPDDR3 DRAM is a natural extension to the low power family of DRAM. The R+LPDDR3 DRAM is optimized for mobile applications and is fully-compliant with industry LPDDR3e/ LPDDR3 specifications. When paired with an R+ LPDDR3 PHY, the DRAM supports data rates of up to 2133 Mbps, while providing an active power reduction of up to 30% when compared to a standards-only LPDDR3 device at equivalent speed.

The improvement in power consumption is due in part to the use of Low Voltage Swing Terminated Logic (LVSTL) signaling technology that features a significantly reduced signal swing versus the 1.2 volt HSUL (High Speed Unterminated Logic) signal swing of LPDDR3. By supporting both signaling types, the R+ LPDDR3 DRAM offers an enhanced performance, low-power mode while maintaining compliance with LPDDR3e and LPDDR3 standards and specifications.

- IO pads
- PLL
- Power Mode Management (PMM)
- Transmit and receive paths
- Clock distribution
- Control logic
- Power distribution
- Electrostatic discharge (ESD) protection circuitry

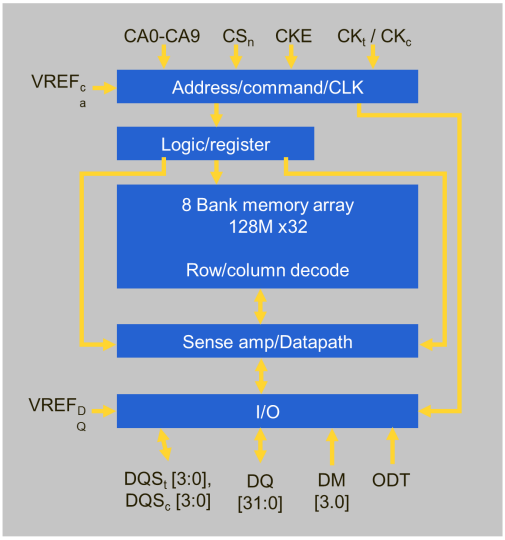
Highlights

- Fully-compliant with JEDEC-standard LPDDR3 and LPDDR3e
- R+ enhanced mode maintains compatibility with existing infrastructure while improving data rate or power consumption
- Up to 30% lower DRAM active power (IDD4R) versus standard LPDDR3
- Supports data rates up to 2133 Mbps and 8.5 GB/sec bandwidth per device
- Compatible with standard LPDDR3 PHYs

Compatibility and Features

FEATURES	LPDDR3	LPDDR3e	R+ LPDDR3
Signaling	HSUL	HSUL	LVSTL
Max Data Rate (Mbps)	1600	2133	2133
Density (Gb)	4 / 8 / 16 / 32	4 / 8 / 16 / 32	4 / 8 / 16 / 32
Data Path Width	x16 / x32	x16 / x32	x16 / x32
VDD1 / VDD2 / VDDQ (V)	1.8 / 1.2 / 1.2	1.8 / 1.2 / 1.2	1.8 / 1.2 / 1.2
Rank Support	2	2	2
Package	POP, FCP, FBPG	POP, FCP, FBPG	POP, FCP, FBPG

R+LPDDR3 DRAM Functional Diagram



Features

- Fully-compliant with industry standard LPDDR3e and LPDDR3
- Compatible with standard LPDDR3 PHYs. No memory controller changes required
- Scalable architecture supports data rates up to 2133 Mbps and 8.5 GB/sec bandwidth per device
- Flexible packaging options (POP, MCP, FBGA)
- Full compatibility to LPDDR3e/LPDDR3 low-power states
- Support data path widths of 16 and 32 bits
- DRAM densities from 4Gb to 32Gb
- Dual rank support
- LVSTL signaling mode available to enable data rates of 2133 Mbps and beyond. No system hardware changes needed to support LVSTL
- Up to 30% lower DRAM active power
- Up to 25% lower active memory system power
- Deep power-down support
- Refresh, self-refresh, and partial array self refresh support
- On-die programmable VrefDQ generation
- Programmable output impedance, on-die termination, and periodic ZQ calibration
- CA eye training, DQS write leveling and DQ read calibration support
- On-Die-Termination support

Engagement Options

Memory Suppliers/Manufacturers

- Complete specification and implementation package
- Reference design database including schematics and matching layout
- Integration guidelines
- Package and PCB design guidelines
- Logic and power simulations
- Timing verification environment
- Device characterization and test environment
- Optional design integration and bring-up support services

SOC/ASIC developers

- Contact R+ LPDDR3 DRAM supplier for datasheet, roadmap, schedule, and pricing
- Contact Rambus for R+ LPDDR3 PHY information

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