R+LPDDR3 PHY

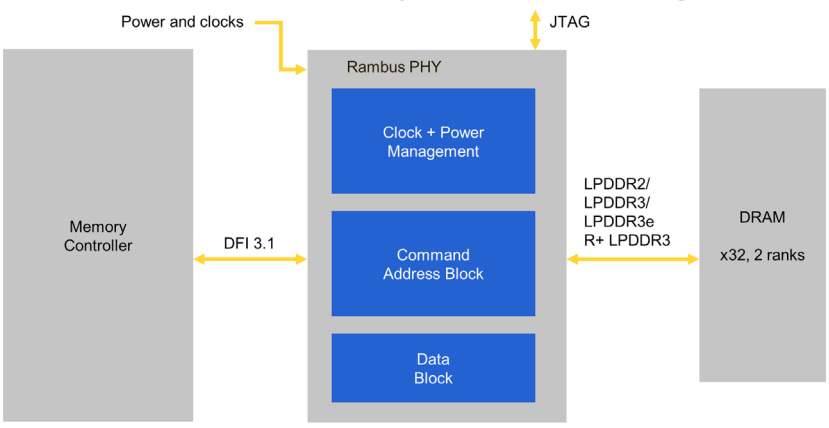
Enhanced performance and up to 25% lower active memory system power for mobile applications, while maintaining compatibility with standard LPDDR3.

Overview

Fully compliant with LPDDR3 and LPDDR2 DRAM specifications, our R+™ LPDDR3 PHY pairs with the R+ LPDDR3 DRAM to create a memory subsystem that supports data rates of up to 2133 Mbps, and reduces active memory system power by up to 25% and active DRAM power by up to 30%. This enables a significantly improved thermal profile and an increased battery life in the end device. The improved thermal profile also enables the memory system to run at peak bandwidth for longer periods of time, which translates to better overall performance in the end systems.

The improvement in power consumption is a result of Low Voltage Swing Terminated Logic (LVSTL), a single-ended, ground-terminated signaling technology, used while in R+ mode. LVSTL features a significantly reduced signal swing versus the 1.2 volt HSUL (High Speed Unterminated Logic) signal swing of standard LPDDR3. Reduced signal swing translates to significantly reduced IO power at high data rate, which is a major component of DRAM power. By supporting LVSTL and HSUL signaling, R+ LPDDR3 offers a low-power mode while maintaining compatibility with LPDDR3 and LPDDR2 DRAM standards.

LPDDR3 PHY Subsystem Example

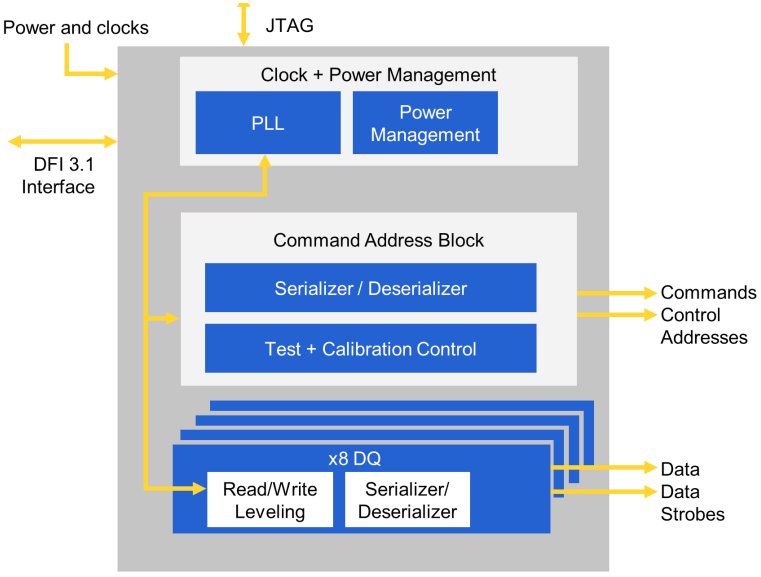


Highlights

- Multi-modal support for R+ LPDDR3, LPDDR3e, LPDDR3, and LPDDR2
- DFI 3.1 and JEDEC standards compliant
- Multi-modal HSUL and LVSTL for data pins
- Supports package-on-package (PoP) and discrete packaging options
- Up to 30% lower DRAM active power (IDD4R) and 25% lower active memory system power versus standard LPDDR3
- Available option with LabStation™ Validation Platform for enhanced bring-up and validation

Standards	Data Rates (Mbps)
R+ LPDDR3	200-2133
LPDDR3e	200-2133
LPDDR3	200-1600
LPDDR2	200-1066

R+ LPDDR3 PHY Configuration



Features

- Socket compatibility to existing PoP, MCP, C2C mobile memory standards
- Full compatibility to LPDDR3 low power states
- Support for x32 channel configuration
- Support for up to 2 ranks
- PLL-based clocking with internal clock alignment to PCLK to reduce power consumption
- DFI 3.1 compliant for easy integration with memory controller
- Multi-modal support for HSUL and LVSTL
- Autonomous initialization
- Selectable low-power operating states
- Programmable output impedance, on-die termination, and periodic ZQ calibrations implemented to improve the signal integrity of the channel
- Utilizes standard 8-layer 6020 metal layer stack
- North-South and East-West configurations available
- Register interface for state observation
- Test traffic generation and error checking for in-situ test
- LabStation™ software environment for system level bring-up, characterization, and validation

Engagement Options

Fully-characterized hard macro (GDSII)

Complete design views:

- Gate-level and IO models
- Verification test benches
- Layout abstracts (.lef)
- Timing models (.lib)

Full documentation:

- Datasheet
- Integration guidelines
- Package and PCB design guidelines
- ASIC/DFT manufacturing guidelines
- Test and characterization user guide
- Verilog models
- CDL netlists (.cdl)
- ATPG models
- GDSII layout
- DRC & LVS reports

Optional design integration and bring-up support services

rambus.com/ddrnphys