



# Protecting Consumer Electronics

Benjamin Jun | Cryptography Research, Inc. | 8 April 2008 | HT1-108



CRYPTOGRAPHY RESEARCH

RSA CONFERENCE 2008

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## Protecting consumer electronics

- Consumer electronics threats
- Learning from open-source

- Probing tools
- Information leakage
- Fault induction
- Boot attacks

## Consumer electronics threats

- Obtain “unauthorized” access to asset
  - Pirated digital content

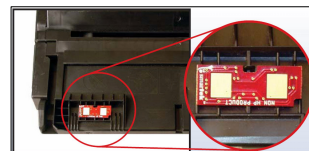


## Consumer electronics threats

- Obtain “unauthorized” access to asset
  - Pirated digital content
- Interact with “unauthorized” device/service
  - Use of non-authentic peripheral



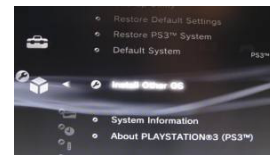
“RAZR V3” Battery



Unauthorized toner chip

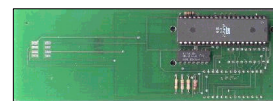
## Consumer electronics threats

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- Make device execute “unauthorized” code
  - Enable unauthorized features, linux



## Consumer electronics threats

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  - Pirated digital content
- Interact with “unauthorized” device/service
  - Use of non-authentic peripheral
- Make device execute “unauthorized” code
  - Enable unauthorized features, linux
- Clone a device
  - Unauthorized copy



Pay TV smartcard emulator

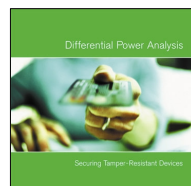


Starting car w/ DST simulator

Source: "Security Analysis of a Cryptographically-Enabled RFID Device", Bono, Green, Stubblefield, Juels, Rubin, Szydio, 1/29/2005

## Who am I? What do I do?

- Cryptography Research, Inc.
  - Solve fraud, piracy problems
  - R&D emphasis on applied security issues
- Design and evaluation services
- License security technologies



DPA:  
Tamper Resistance



CryptoFirewall:  
Pay-TV Security



SPDC / BD+:  
Renewable Security  
for Digital Content

**Try this at home!**

***Learn from open-source embedded projects***

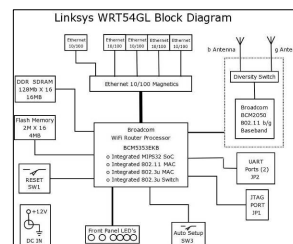
## Looking to open-source embedded projects

- Not (really) a security compromise...
  - Learn about techniques to gain control of and use HW
  - Reverse engineering is a key part of project efforts
- Good engineering lessons
  - Fast way to explore deployed embedded environments
  - Good fun! Good return on \$ + time.



## Linksys WRT54GL

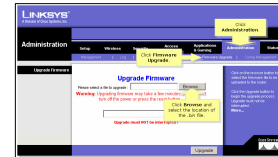
- \$60 home wireless router
  - Linksys released open source SW (2003)
- Why modify?
  - Modify operating parameters (xmit power, etc.)
  - Add more firewall settings, mesh networking, QoS, use metering, etc.
  - Linux on cheap, low power platform
- Thriving hobbyist community
  - DD-WRT ([www.dd-wrt.com](http://www.dd-wrt.com))
  - OpenWRT ([www.openwrt.org](http://www.openwrt.org))
  - Note: buy the WRT54GL



Linksys (Cisco Systems)  
The Consolidated Hacking Guide For The Linksys  
WRT54GL, "ByteEnable", [www.linuxelectronics.com](http://www.linuxelectronics.com)

## FW reflash of Linksys WRT54GL

- Example: Upgrade to OpenWRT firmware
  - Download OpenWRT whiterussian rc5, squash fs  
<http://downloads.openwrt.org/whiterussian/rc5/bin/openwrt-wrt54g-squashfs.bin>
  - Use (unsecured) firmware update mechanism
  - Router reboots, use www interface to set root pw
  - SSH in!



Stock Linksys FW: "4.30.12 1/10/2008"

OpenWRT FW: whiterussian rc5, squash FS

ASCII: "W54G"      Build date: 2007 Dec 14      Version 4.30.12      32-bit CRC

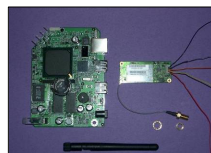
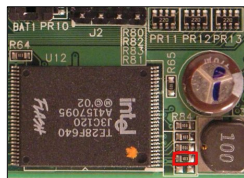
```

openwrt-wrt54g-squashfs.bin
00000000  47 35 34 47 00 00 00 00 06 03 10 04 14 00 55 32  UC4S.....U2
00000010  4E 31 00 00 1F 00 00 00 00 00 00 00 00 00 00 00  ND.....
00000020  48 44 52 30 00 60 17 00 6C B2 BE D0 00 01 00 00 00  HDR0...l....
00000030  1C 00 00 00 08 08 00 00 C4 07 00 1F 8B 08 00 00 00  ....VAl.i....
00000040  00 00 00 00 02 03 A5 56 41 6C 1B 15 15 FE FC CF  sq.L.....8V.
00000050  24 71 D2 03 4C 1C B7 9A 96 7A 9A BF 9E 38 56 B3  V.*V.....l.=
00000060  A0 53 D6 2A 52 43 83 FD AF 72 FB 21 A4 3D E4
  
```

ASCII: "HDR0"      Offset to start of kernel from .TRX header

## Try this: NSLU2

- Linksys NSLU2
  - Ethernet SMB (Windows) fileserver for USB disks (\$70)
- NSLU-linux project ([www.nslu2-linux.org](http://www.nslu2-linux.org))
  - Unslung distribution keeps stock Linksys functionality
  - Disk makes it easy to experiment with
- HW mods
  - Overclocking, serial port, RAM upgrade, debug ports, etc.



<http://www.nslu2-linux.org/wiki/HowToAddAThirtyFourPinUniversalConnector> <http://www.nslu2-linux.org/wiki/HowToOverClockTheSlug> David Hicks, <http://www.nslu2-linux.org/wiki/HowToAddInternalWireless>

## No surprise to embedded developers...

- Nearly all products based on commodity cores, reference designs
  - WRT54GL: Broadcom BCM5352E
  - NSLU2: Intel IXP420 XScale (ARM)
- Small number of widely used embedded development environments
  - Linux, uC Linux, VxWorks
  - Good development, cross-compilation, debugging tools
- Hardware is incrementally “free”
  - Differentiating features governed by software
  - Software modifications have interesting results!



## Why follow these projects?

- Infrastructure type projects
  - “Boot linux on \_\_\_\_ platform.”
  - Understand debugging, porting tools
- Patch type projects
  - “Get in, get system to do \_\_\_\_, get out.”
  - SW reverse engineering
- Hardware extension projects
  - HW reverse engineering

## Probing

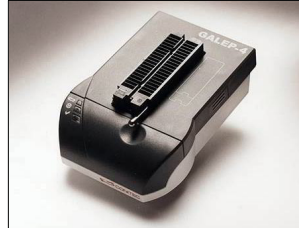
### Probing goals

- Goal: Gather enough information for analysis
  - Reverse engineering is about making hypotheses
  - ... and finding ways to confirm them !
- Static analysis
  - Use disassemblers and static analysis tools
- Probe system as it responds to stimuli
  - In normal processing
  - In abnormal processing



## Static reading of flash / ROM

- For discrete parts, this is easy...
  - Use ROM reader
  - Tap data bus, drive address bus
- On-die ROM
  - Get software to read it!
- With a code dump...
  - Recognize processor type
  - Disassemble, probe for implementation weakness
  - Search for keys (high entropy)



Conitec GALEP-4 programmer/reader

```
FW_WRT54GL_4.30.12.3_US_EN_code.bin
00000000 57 35 34 47 00 00 00 00 0C 14 04 1E 0C 55 32 W54G.....U2
00000010 4E 44 00 00 1F 00 00 00 00 00 00 00 00 00 00 ND.....
00000020 48 44 52 30 00 E0 2C 00 F3 9F DA C3 00 00 01 00 HDR0.....
00000030 1C 00 00 00 30 B9 0A 00 00 00 00 00 1F 8B 08 08 .....0.....
00000040 08 1E 6A 47 02 03 70 69 67 67 79 00 EC 7D 0D 74 ..jG..piggy..}..t
00000050 1C 57 95 E6 ED 57 DD 52 DB 6E C7 25 A9 2D B5 6D W...W.R.n.%-..m
00000060 25 FE 96 4B 3F B1 45 F8 04 25 68 98 5E A8 B4 E5 % K? E %h ^
```

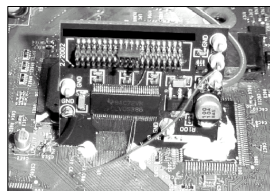
## Probing tools



IC test clip (PLCC)  
*Emulation Technology Part 5281*



SCSI Bus Analyzer  
*Cryptography Research*



Custom FPGA Logic Analyzer  
*Bunnie Huang, <http://www.xenatera.com/bunnie/proj/anatak/xboxmod.html>*



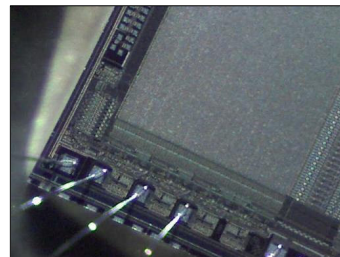
GPIB Oscilloscope + Logic Analyzer  
*Agilent Technologies, 1672G data page*

## Countermeasures to probing

- Bury vias
  - “Production” mode harder, one-time probing still doable...
- Use “encrypted” memory
  - Use global or unique key
  - If keys managed by SW, this is essential
  - ... but difficult to rely on with many copies of identical data
- Hardcode keys + algorithms + processing
  - Integrity + privacy benefits
  - Good: In SoC ROM
  - Better: In HW gates

## Die imaging: ROM

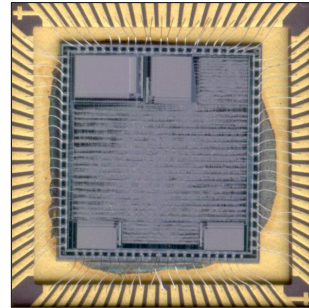
- Imaging on-die ROM
  - Optical microscope / FIB: Use automated tool to image ROM
  - Active probing: Tap data bus, drive address bus
  - Passive probing: Tap bus lines
- Responses
  - Shield metal layers
  - “Encrypted” memory
  - HW-based obfuscation



Memory image: Hector Vega  
FIB: University of Cambridge Department of Materials Science Device Materials Group

## Die imaging: Gates

- Imaging attacks on gates
  - Automated tool to image + recover netlist
  - Easier if crypto area small, design has good structure
  - One reference: Nohl, Starbug, Plotz, *Mifare Security*, CCC 2007
- Responses
  - Shield layers
  - Camouflage libraries
  - If imaging not 100% accurate...



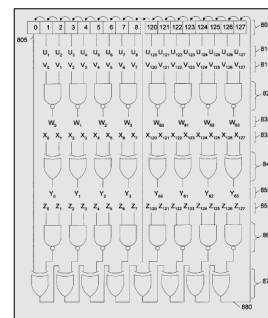
### Step 2: Encircle Crypto

- Even tiny RFID chip too large to analyze entirely
- Crypto <10% of gates!
- Focus on interesting-looking parts:
  - Strings of flip-flops (registers)
  - XOR
  - Units around edges that sparsely connected to the rest of the chip

[http://www.ece.cmu.edu/~koopman/stack\\_computers/binar\\_chip.jpg](http://www.ece.cmu.edu/~koopman/stack_computers/binar_chip.jpg)  
Nohl, Starbug, Plotz, *Mifare Security*, CCC 2007

## Example: Entropic Array

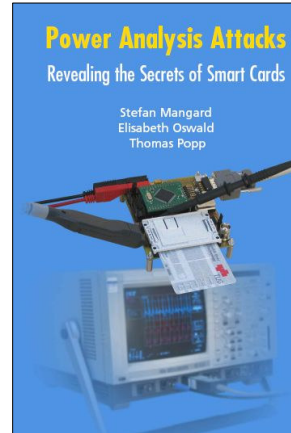
- State-of-the-art reverse engineering techniques are error-prone
  - Attacks involve human interpretation + correction
  - For normal circuits, attackers do fine w/buggy output
  - Example: AES with a few errors is obviously AES
- Goal: make imperfect reverse engineering results useless
  - Exact circuit required to perform crypto correctly
    - Attackers can't infer where they made mistakes
  - EA designed to be difficult to interpret
    - "Grown" from design rules and random seed
    - Internal entropy / lack of structure



Example EA

US patent 6,640,305

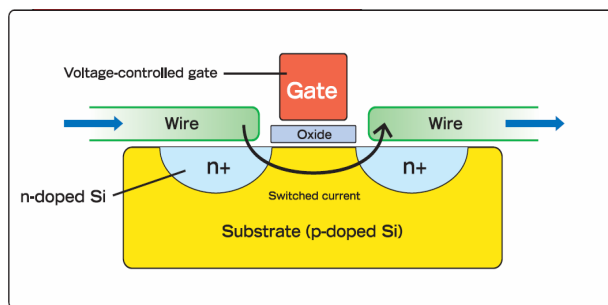
## Information Leakage Attacks



Mangard, Oswald, Popp  
[www.dpabook.org](http://www.dpabook.org)

## Information leakage

Integrated circuits consume power as they operate.



Typical MOS Transistor

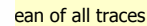
## EXPONENT!



**SQUARE**

## CONDITIONAL MULT

## RSA CONFERENCE 2008



select guess  $g$  for  $K_i$

rect guess  $g$  for  $K$ .

- 

## Hybrid attacks

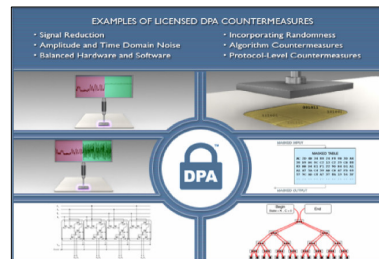
- Use power consumption as an output channel



- Code insertion
  - Buffer overflow loads + executes target code
- For each bit of data
  - Perform instruction A or instruction B 256 times
  - Dump memory via SPA activity

## Defenses against power analysis

- Categories
  - Obfuscation
  - Leak Reduction
  - Balanced HW / SW
  - Amplitude & Temporal Noise
  - Incorporating Randomness
  - Protocol Level CM
- Certifications / Requirements
  - FIPS 140-3 draft
  - Common Criteria
  - CAC, E-Passport, HSPD-12
- Complicated!
  - Naïve CM can make things worse
  - Device evaluation is important



Cryptography Research

Use of these countermeasures requires a license from Cryptography Research and is protected under US patents 6,278,783, 6,298,442, 6,304,658, 6,327,661, 6,510,518, 6,539,092, 6,654,884 and other patents issued and pending in the US and worldwide

## Fault Induction Attacks

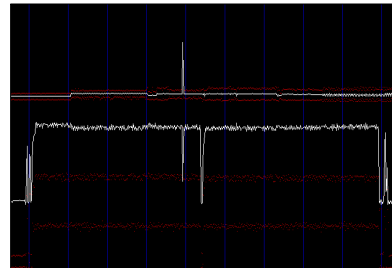


Van de Graff (left)

US Smithsonian Institution

## Why induce faults?

- Security code (generally) assumes that platform is reliable
  - What if it isn't?
- Why do this?
  - Induce a computational fault
  - Change value being read/stored
  - Break into/out of an execution loop
  - Change program counter (PC)
- Surprises
  - More repeatable than you think...

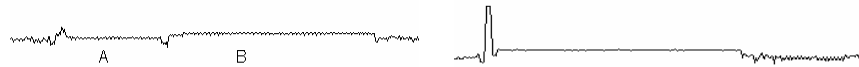


Glitch impulse & power trace during successfully-glitched RSA CRT

Cryptography Research, Inc.

## Tearing nonvolatile memory writes

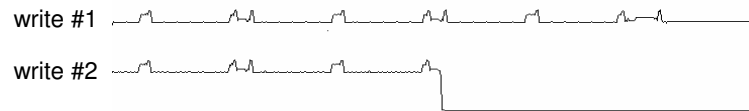
- Typical EEPROM write/clear cycles



Device 1: Bit Clearing Phase (A) and Bit Setting Phase (B)

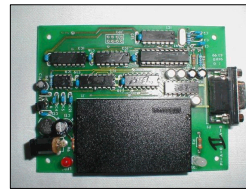
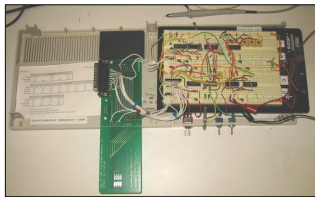
Device 2: Bit Setting Phase (A) and Bit Clearing Phase (B)

- Tearing example



Cryptography Research, Inc.

## Glitching tools





## Glitching examples

- Glitch instruction to extend output loop
  - Example: DJNZ instruction

```

; This routine is used to output a 4-byte result
; DPTR points to first byte of data
result_out: MOV R0, 3          ; set loop counter
result_loop: CALL #putch       ; call UART routine
              INC DPTR         ; increment pointer
              DJNZ R0, #result_loop ; conditional loop
              RET

```

- Glitching program counter
  - “Serpent’s tail”: NOP sled followed by target code

## Example glitch defenses (SW)

- Check your work!
  - Verify private key computations
- Preincrement error flags

Before

```

// check password
result = secureMemCmp(passwordLen, userPin, userInput);
if (result)
    nvmeErrorCount = 0;
else if (++nvmeErrorCount > errorMax)
    lockOut();
return (result);

```

After

```

if (nvmeErrorCount++ > errorMax)
    lockOut();
result = secureMemCmp(passwordLen, userPin, userInput);
if (!result)
    nvmeErrorCount = 0;
return (result);

```

## Example glitch defenses (HW)

- Environmental sensors
  - Monitor clock, voltage
  - Not available in all silicon processes
- Independent votes
  - Independent modules vote before enabling output, unlock
- Canary logic (CryptoFirewall)
  - Cumulative hash of system control state on every clock
  - Hardware design element designed to be on critical path
  - Example: Gate output unless canary logic permits operation



Canaries used to detect CO gas in mines  
(Hollinger Mine, Ontario, 1928 )

## Boot Attacks



*"Let's start at the very beginning  
A very good place to start  
When you read you begin with A-B-C  
When you sing you begin with do-re-mi"*  
– Maria

Rodgers, Hammerstein, *The Sound of Music* (1965)

## Taking over a device

- Step 1: Understand how device operates
- Step 2: Get (malicious) code on the device
- Step 3: Get control of program counter (PC)

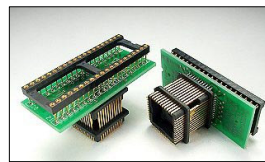
37

## Getting to execution – ROM/flash replacement

- Socketed flash/ROM



BIOS socket (X-Box)  
*Bunnie Huang, xenatera.com*

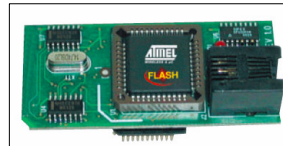


DIP to PLCC adaptor  
*Logical systems, www.logicalsyst.com*

- ROM / flash emulator



ROM emulator  
*Transtronics Pocket ROMulator*



Flash emulator  
*MSC AT51Flash-Emulator*

## Getting to execution – debug tools

- JTAG analyzer
  - Full debug interface
  - Boot code replacement
  - In-target flash/ROM reading + programming



EJTAG In-target analyzer  
*First Silicon Solutions, ISA-MIPS*



ARM JTAG debugger interface  
*Olimex Ltd., ARM-USB-OCD*

## Getting to execution – taking over control

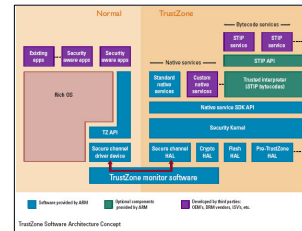
- Take over control directly
  - Buffer overflow, glitch to executable code, protocol errors, ...
  - Suspend/resume with memory image change
- Bypass authentication in bootloader
  - Bypass authentication process (CRC, signature)
    - Common problem: bad authentication protocol
  - Ex: "Savegame" buffer overflow in "007" Xbox game (2003)
    - Modifies public key, makes modulus divisible by 3
    - Signature forgery, clean start sequence!

```
BE00000080    mov esi, 80000000
AD           lods     ; 0x00000032
$1EE0300000    sub esi, 00000003
3DBD1B4BA4    cmp eax, A44B1BBD
75F2           jne 00000032 ; scan RAM for public key
$176FFD68BD72D xor dword ptr [esi-0], 2DD78BD6 ; modify last 4 bytes of public key
```

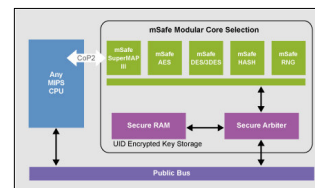
<http://xbox-linux.sourceforge.net/docs/007analysis.html>

## HW tools for boot protection

- **ARM TrustZone**
  - Lightweight hardware extensions for security
    - S-Bit added to CP15 register
    - SMI (Secure monitor interrupt) instruction
  - Only privileged OS can issue SMI
  - Non-secure processes have limited privileges
- **MIPS Safe-SOC**
  - Peripheral on MIPS coprocessor bus
  - Crypto accelerator with access to memory space
- **Cautions**
  - Monitor and secure kernel should be small
  - Watch out for complexity!



ARM TrustZone Architecture



MIPS Safe-SOC Architecture

ARM, MIPS product literature

## Example: Bootloader with code signatures

- Boot ROM with code authentication
    - Reset vector jumps to boot ROM
    - Verify RSA cert (hash of PK can be hard-coded)
    - Hash and verify payload, FAIL on error
    - Decrypt + decompress payload to RAM
    - Clear all other RAM
    - Jump to payload
- HW requirements
    - Force jump to internal boot ROM on reset
    - JTAG and other execution vectors should be off on boot
    - Development/test: skip bootloader if fuse unblown



## Example: Continuous code checking

- Continuous verification
  - Boot ROM starts watchdog timer
  - Background code scanning process
    - Steps through program RAM & computes hash
    - Restart timer if code check passes
  - Code scanning is interruptible
    - Halt & restart completely if interrupted
    - Can work on smaller chunks of code
      - Verify one branch of a hash tree at a time
- HW requirements
  - Watchdog that can only be started by code in boot ROM area
  - Requires protected RAM or dirty bit that is set on interrupt

## Bootloader challenges

- Challenges
  - Enabling development environment
  - Support for powerdown / sleep modes
  - MMU behavior as system boots
- “Cat and mouse”
  - Example: smartcard code hashing and emulators



Checkpoint Charlie (1986)

## Where do we go from here?

### Conclusion

- Most consumer electronics devices:
  - Are in physical possession by attacker
  - Have flat memory architectures
  - Are used offline
- Developer tools == attacker tools
  - Most systems use standard platforms + tools
  - Good debuggers and debugging interfaces
- HW and SW can't do this alone!
  - SW can enable functionality, handle updates
  - HW can enforce small set of rigid rules



## Contact Information

For more information, or to discuss how Cryptography Research can help with a security problem:

Benjamin Jun  
ben@cryptography.com  
415.397.0123  
www.cryptography.com



## We're hiring!

If you are technically strong and want to work on challenging crypto and security problems, please send a resume!

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