Rambus

MEMORY + INTERFACES
R+ Serial Link PHYs
Product Brief

R+1.25-16 Gbps Multi-protocol Serial Link PHY

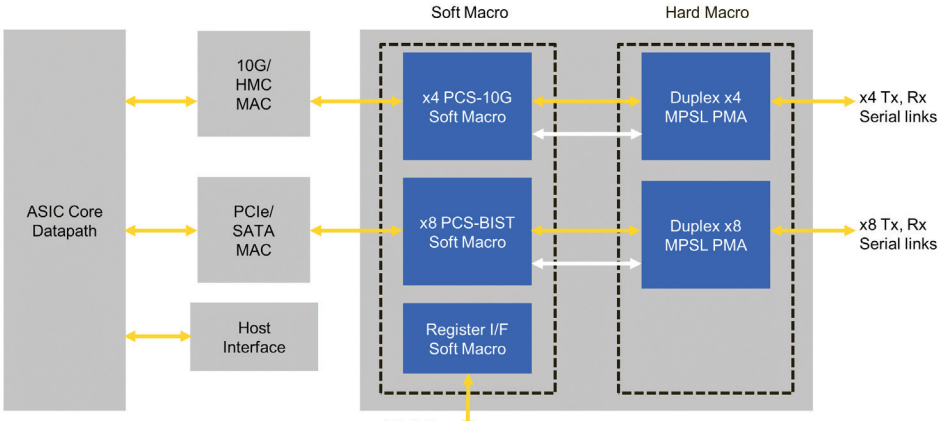
Designed to maximize interface speed with broad protocol compatibility speed in the difficult system environments found in enterprise-class applications.

Overview

The Rambus R+™1.25–16 Gbps Multi-Protocol Serial Link (MPSL) is a complete solution designed with a system-oriented approach to maximize flexibility and ease integration for our customers. It is optimized for power and area in difficult, high-loss channels and utilizes FIR, CTLE, and DFE equalizers to recover data in the presence of channel and system interfaces. Our R+ 1.25–16G MPSL is designed with a minimal set of broadside control and status pins, as well as a soft-configurable PCS, to support a wide range of applications including:

- Gigabit Ethernet copper backplane networking
- XFP and SFP+ optical modules
- System packet interfaces
- Hybrid Memory Cube
- TDM Fabric to Framer interface
- Graphics cards
- PCIe peripheral connectivity
- Server connectivity

1-16G MPSL PHY Subsystem Example



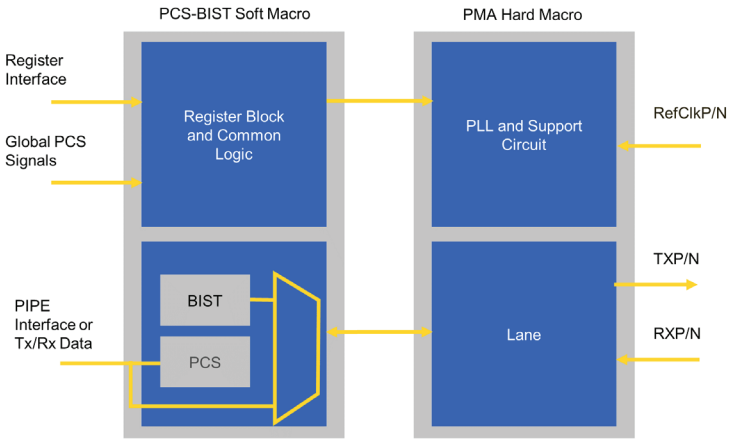
Highlights

- PMA hard macro optimized for PCIe, SATA, 10G/CEI/Interlaken, HMC, Fibre Channel & JESD204 interfaces
- PCS soft macro for PCIe (PIPE4.2 compliant) and 10G-KR connectivity to controller macro
- x1, x2, x4, and x8-lane configurations
- BIST with PRBS generator and checker
- Tx and Rx equalization
- Data rate negotiation
- Equalization adaptation

Protocol Compatibility

Protocol	Data Rates (Gbps)
PCIe	2.5, 5, 8, 16
SATA	1.5,3,6
SAS	3, 6, 12
10GBase-KR	10.3125
1000Base-KX	1.25
10GBase-KX4	3.125,6.25
XAUI/2xXAUI	3.125, 6.25
CEI6-SR	4.976-6.375
CEI11-SR, LR	9.95-11.2
XFI	9.95-11.2
Interlaken 6 G & 10 G	4.976-6.375, 10.3125
HMC 2.0	15
Fibre Channel	4.25/8.5/14.025
JESD204C/B	12.5-16.3
CPRIv5,6	1.2288-10.1376

R+ 1-16G MPSL PHY Configuration



Features

- Duplex lane configurations of x1, x2, x4, and x8
- Transmit swing of at least 800 mV differential peak-to-peak for MR & LR, 360mv for SR
- Support for AC-coupled interfaces
- Fine-grain power up/down capability for power optimization, and ability to turn off unused link(s)
- BER of 10^{-15} for CEI11-LR/SR and BER of 10^{-12} for SFI, XFI, PCIe and GbE protocols
- A wide range of PLL multiplication options supporting low reference clock frequencies
- Flexible ASIC clocking
- Tight skew control of 2UI between lanes of the PMA
- 3-tap Tx Finite Impulse Response (FIR) equalizer with multi-level de-emphasis
- Deterministic latency with in +-1UI variation for Tx lane
- Continuous time linear equalizer (CTLE) with programmable settings providing up to 12dB gain peaking at Nyquist frequencies
- 6-tap Rx DFE (decision feedback equalizer)
- Second-order CDR meeting SSC and RX sinusoidal jitter requirements
- Expandable register interface enabling communication with multiple PMAs and PCS-BIST soft macros
- Built-in Self Test (BIST) with ATPG and AC/DC Boundary scan support
- Built-in PRBS pattern generation and checking for standalone loopback testing
- In-situ real-time monitoring and receive data eye schmoo
- Operation across a wide temperature range (-40 C to +125)

Deliverables

PMA Hard Macro

- Verilog models
- LEF abstracts (.lef)
- Timing models (.lib)
- CDL netlists (.cdl)
- ATPG models
- IBIS-AMI models
- GDSII layout
- DRC & LVS reports

PCS-BIST Soft Macro

- RTL model

Datasheet

SoC integration guide

Optional design integration and bring-up support services

rambus.com/seriallinks