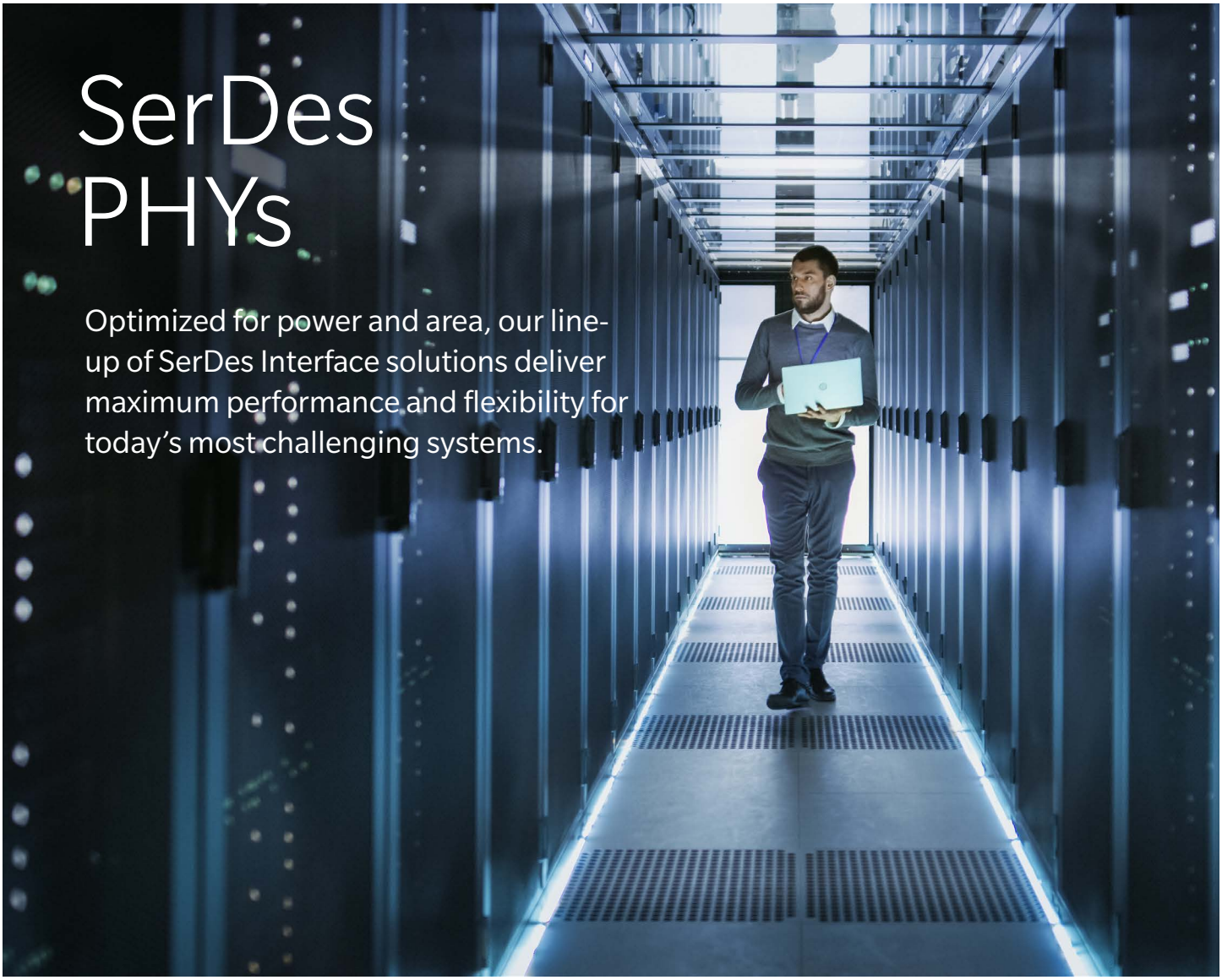
Rambus



# SerDes PHYs



Optimized for power and area, our line-up of SerDes Interface solutions deliver maximum performance and flexibility for today's most challenging systems.

## Fully Standards-Compatible

- Faster time-to-market
- Multi-protocol support

## Enhanced Design Flexibility

- Flexible packaging options
- Improved margin and yield

## Reduced Power

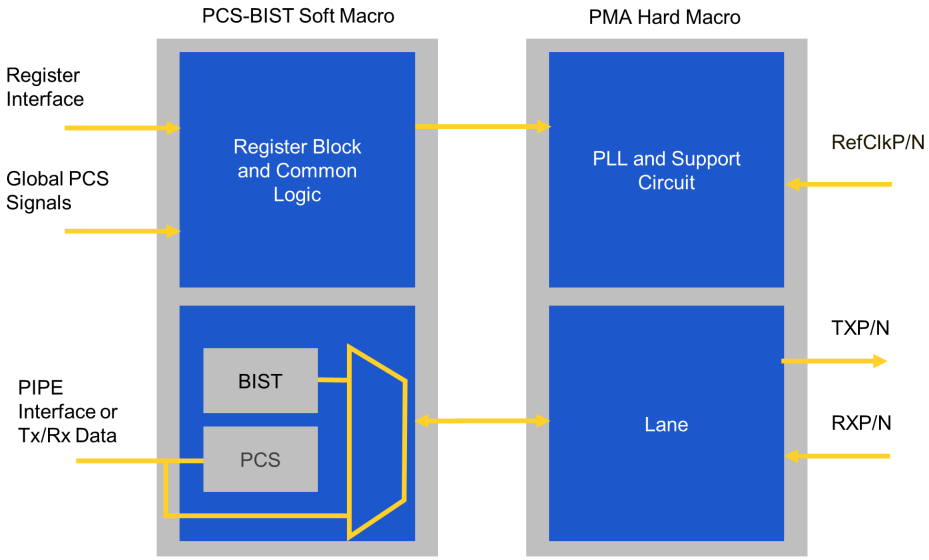
- Wide range of PLL clock multipliers
- Fine-grain power -up/down options

## Overview

Our SerDes interfaces are high-quality, complete PHY solutions designed with a system-oriented approach to maximize flexibility and ease integration for our customers. Optimized for power and area at peak bandwidth, SerDes PHYs enable differentiation while maintaining compatibility with industry standards.

The SerDes interface family includes a range of solutions to meet a variety of speed and application requirements. The family of solutions includes:

- 112G Multi-protocol SerDes PHY
- 56G Multi-protocol SerDes PHY
- 32G Multi-protocol SerDes PHY
- 28G Multi-protocol SerDes PHY
- 16G Multi-protocol SerDes PHY
- 12G Multi-protocol SerDes PHY




We offer complete PHY solutions – our SerDes PHY includes a Physical Media Attachment (PMA) hard macro and Physical Coding Sub-layer with Built-in Self-Test (PCS-BIST) soft macro. The PHYs can also be configured to multiple channel widths and packaging options, which simplifies integration and maximizes design flexibility.

## Features

- Available in 7nm, 14nm, 28nm and 40nm FinFET process nodes
- PMA hard macros optimized for multiple protocols including PCIe, SATA, SAS, 400G/CEI/ Interlaken, HMC, Fibre Channel and JESD204 interfaces
- Industry compliant PCS and MAC soft macros
- Support for x1, x2, x4 and x8 channel configurations
- Advanced Tx and Rx equalization
- Equalization adaptation
- BIST with PRBS generator and checker
- Data rate negotiation

## Deliverables

**PMA hard macro**

- Verilog models
- LEF abstracts (.lef)
- Timing models (.lib)
- CDL netlists (.cdl)
- ATPG models
- IBIS-AMI models
- GDSII layout
- DRC and LVS reports
- PCS-BIST soft macro
- RTL model

**Datasheet**
**SOC integration guide**
**Optional design integration and bring-up support services**

rambus.com/serdes