The Impact of Higher Data Rate Requirements on MIPI CSI℠ and MIPI DSI℠ Designs

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Overview

- The trend towards higher resolution, pixel depth and frame rate cameras and displays is driving the need for higher data rate interfaces.
- The MIPI Alliance Camera Serial Interface (CSI) and Display Serial Interface (DSI) standards are evolving to meet these needs.
- This presentation provides an overview of these trends, the evolving standards, and the corresponding impact on CSI and DSI designs.

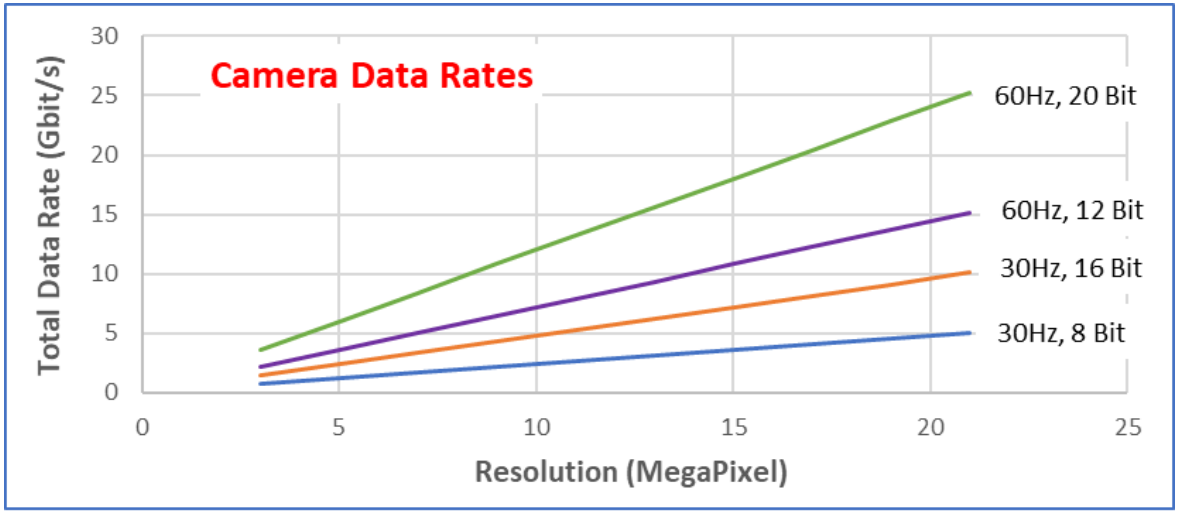
Speaker Introduction

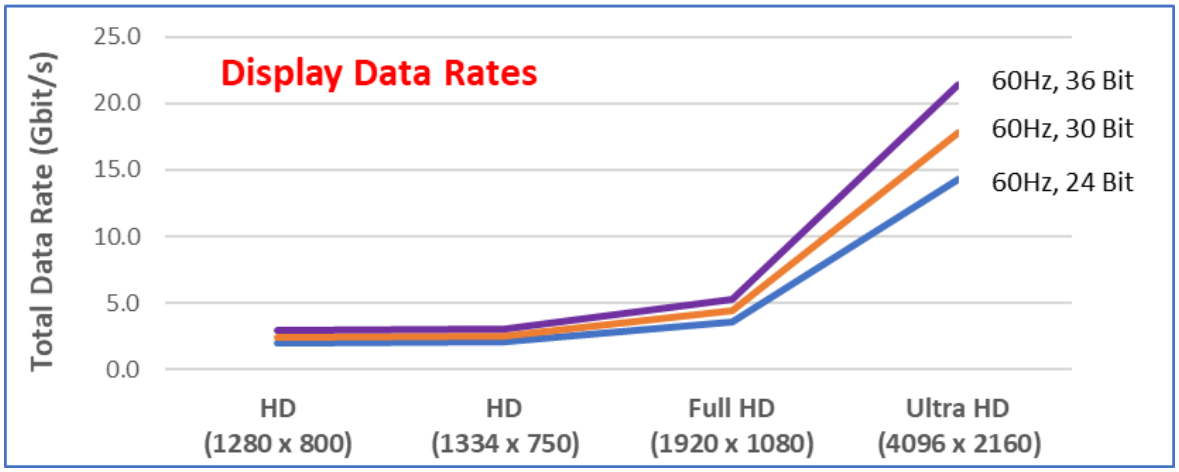
- Brian Daellenbach
  - President of Northwest Logic
  - Located in Hillsboro, Oregon
  - Controller IP Provider – MIPI, PCIe, DDR/HBM
- Ashraf Takla
  - President of Mixel
  - Located in San Jose, California
  - MIPI PHY Provider – D-PHY, C-PHY, M-PHY
- Together Northwest Logic and Mixel provide a complete, silicon-proven, high-performance, low-power MIPI solution

MIPI Standards Background

- MIPI Alliance was formed in 2003 to “to benefit the mobile industry by establishing specifications for standard hardware and software interfaces in mobile devices”
- Camera Serial Interface (CSI)
  - Provides a packet-based protocol for interfacing to mobile cameras
  - Widely used
- Display Serial Interface (DSI)
  - Provides a packet-based protocol for interfacing to mobile displays
  - Widely used
- Widespread adoption of these standards in the high-volume mobile market has resulted in low-cost cameras and displays which are being used in other markets also

Camera & Display Trends





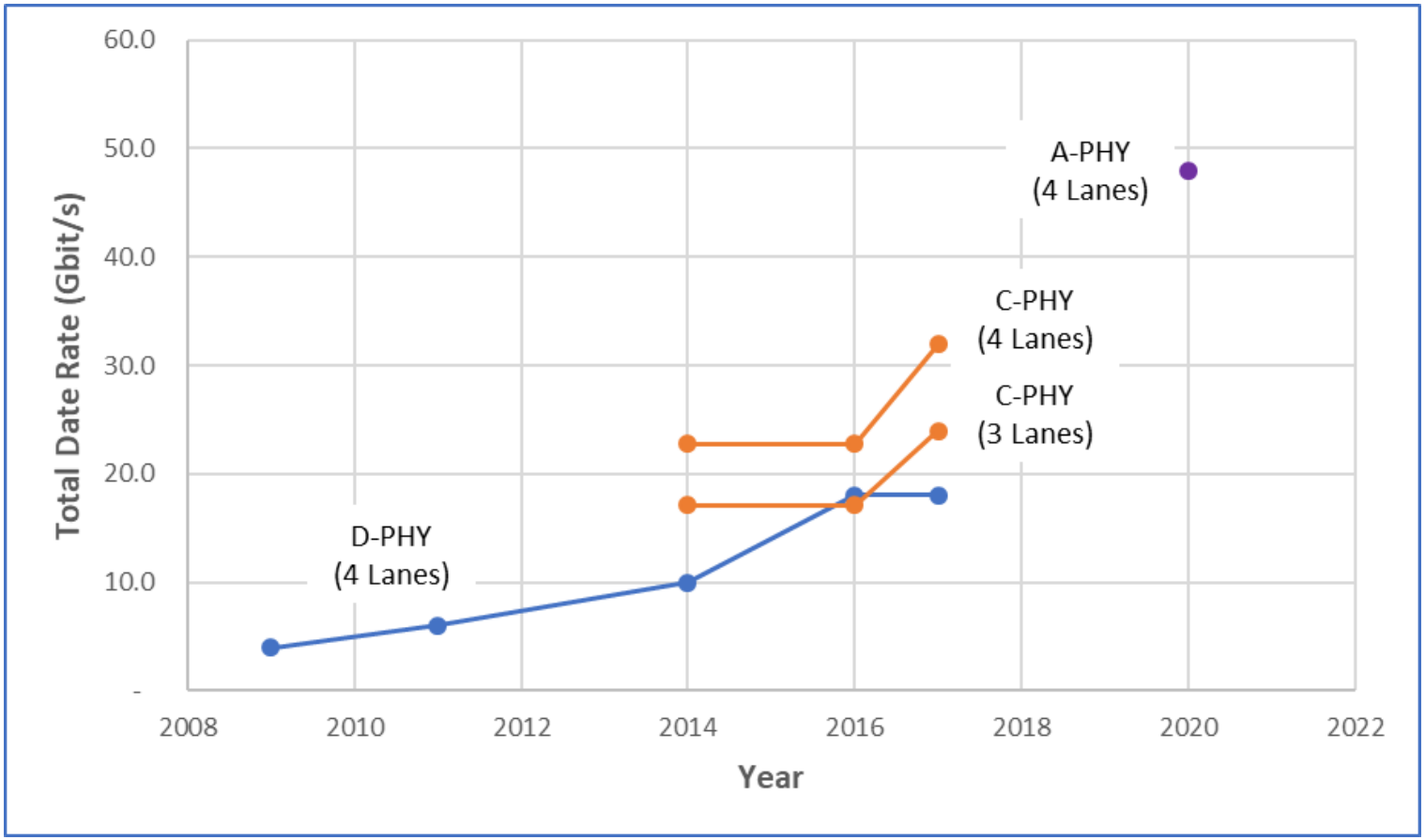
MIPI PHY Standards

- D-PHY
  - N data lanes and 1 clock lane (2 pins per lane)
    - Source synchronous (clock provided separately from the data)
    - Typically 1-4 data lanes are used. 8 infrequently used.
  - Switches between Low Power (LP) and High Speed (HS) modes
    - LP: LVCMOS, HS: Sub-LVDS
  - Widely used in the Camera and Display markets
- C-PHY
  - N data lanes (3 pins per lane – also known as trios)
    - Uses 3 phase symbol encoding (2.28 bits/symbol).
    - Clock embedded in each data lane.
    - Typically 1-3 lanes are used to be pin count compatible with D-PHY. More lanes may be used in the future.
  - Low Power (LP) and High Speed (HS) modes
  - Starting to be used in the Camera and Display markets
- A-PHY
  - Targeted to automotive market. Transmit up to 15 meters. Standard in development.
- M-PHY
  - SERDES-based standard
  - Not being adopted in the Camera and Display markets yet due to higher cost

PHY Standard Roadmap

Standard	Version	Adopted	Data Rate (per lane)	PHY Interface (per lane)	Comment
D-PHY	1.0	Sep 2009	1.0 Gbit/s	8 bit	
	1.1	Dec 2011	1.5 Gbit/s	8 bit	
	1.2	Sep 2014	2.5 Gbit/s	8 bit	
	2.0	Mar 2016	4.5 Gbit/s	8/16/32 bit	
	2.1	Apr 2017	4.5 Gbit/s	8/16/32 bit	
	3.0	Q1 2019	TBD	TBD	
C-PHY	1.0	Oct 2014	2.5 Gsym/s	16 bit	C-PHY lane is known as a Trio. 1 Symbol = 2.28 bits.
	1.1	Feb 2016	2.5 Gsym/s	16/32 bit	
	1.2	Apr 2017	3.5 Gsym/s	16/32 bit	
	2.0	Q1 2019	TBD	TBD	
A-PHY	1.0	Q1 2020	12 Gbit/s	TBD	Can transmit up to 15 meters

PHY Standard Data Rates



CSI-2 Standard Roadmap

Standard	Version	Adopted	PHYs Supported
CSI-2	1.0	Nov 2005	D-PHY 0.58
	1.1	Jan 2013	D-PHY 1.1
	1.2	Sep 2014	D-PHY 1.2
	1.3	Oct 2014	D-PHY 1.2, C-PHY 1.0
	2.0	Mar 2017	D-PHY 2.1, C-PHY 1.2
	2.1	Apr 2018	D-PHY 2.1, C-PHY 1.2
	3.0	Q1 2019	D-PHY 3.0, C-PHY 2.0

DSI-2/DSI Standard Roadmap

Standard	Version	Adopted	PHYs Supported
DSI	1.0	Apr 2006	D-PHY 0.65
	1.1	Nov 2011	D-PHY 1.1
	1.2	Jun 2014	D-PHY 1.1
	1.3	Mar 2015	D-PHY 1.2
DSI-2	1.0	Jan 2016	D-PHY 2.0, C-PHY 1.1
	1.1	May 2018	D-PHY 2.0, C-PHY 1.1
	1.2	TBD	D-PHY 2.1, C-PHY 1.2
	TBD	TBD	D-PHY 3.0, C-PHY 2.0

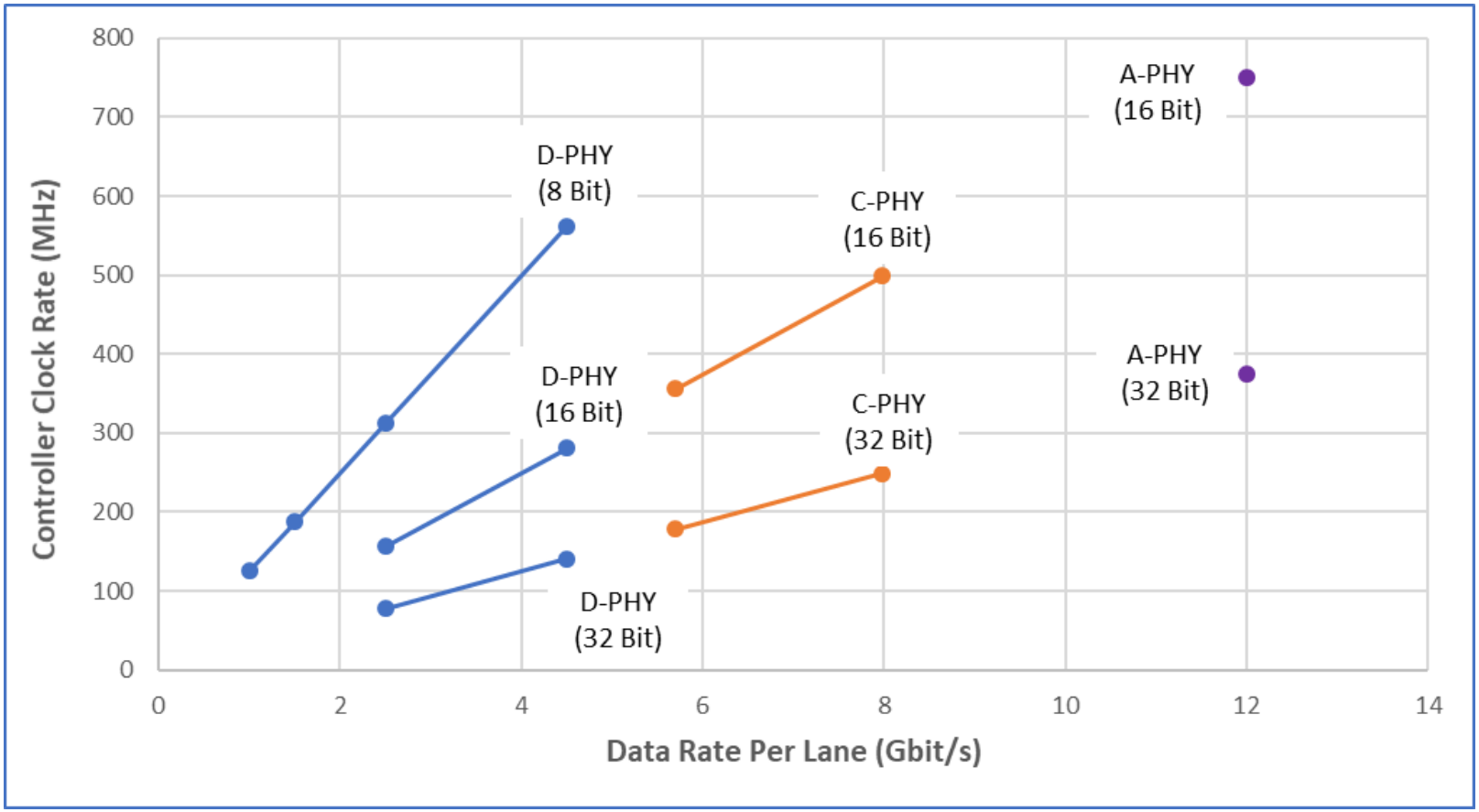
Key Design Impacts

- To keep clock rates reasonable, PHYs are evolving from 8 to 16 to 32 bits/lane
  - PHY data lane rate / PHY data lane width = Controller clock rate
  - Example: 2.5 Gbit/s/lane / 8 bits/lane = 313 MHz clock rate
- This causes the Controllers widths to evolve from 32 to 64 to 128 bit core widths
  - # of lanes * per lane width = Controller core width
  - Example: 4 lanes * 8 bits/lane = 32 bit Controller width
- PHYs and Controllers are starting to support multi-mode D/C-PHY operation

Controller Clock Rates

Standard	Data Rate Per Lane	Clock Rate (8 bit PPI)	Clock Rate (16 bit PPI)	Clock Rate (32 bit PPI)
D-PHY	1.0 Gbit/s	125 MHz		
	1.5 Gbit/s	188 MHz		
	2.5 Gbit/s	313 MHz	156 MHz	78 MHz
	4.5 Gbit/s	563 MHz	281 MHz	141 MHz
C-PHY	2.5 Gsym/s		356 MHz	178 MHz
	3.5 Gsym/s		499 MHz	249 MHz
A-PHY	12 Gbit/s		750 MHz	375 MHz

Controller Clock Rates



Clock Rate Comments

- Most D-PHY 2.0 and C-PHY 1.1 capable PHYs will support 16 bit PPI
  - We expect 8 bit PPI will be phased out
  - We expect some 32 bit PPI to be used
- D-PHY 2.0 and C-PHY 1.1 are more likely to be used in smaller geometry processes
  - Maximum clock rate is likely to be less an issue
    - There may be exceptions to this where a larger geometry, slower LP process is being targeted
- Over next couple of years, D-PHY and C-PHY data rates will continue to push up

Mixel PHYs

- Tracking the standards with several generations of silicon-proven D-PHYs
  - 1.0 Gbps -> 1.5 Gbps -> 2.5 Gbps -> D+C-PHY support
- Support range of PHY configurations
  - D-PHY only, D/C-PHY, C-PHY only, M-PHY
- Broad process support
  - 180nm down to 16nm
- Broad foundry support
  - 7 different foundries including TSMC, UMC, GF, SMIC, and others
- Full featured & differentiated solution
  - Low power, small area, high performance, mature, silicon proven

Northwest Logic Controllers

- First Generation
  - CSI-2 and DSI Controller Cores are 32 bits wide
- Second Generation
  - CSI-2 and DSI-2 Controller Cores support both 32 and 64 bit width
  - 32 bit: minimize size and power for lower data rates
  - 64 bit: minimize clock rate for high data rates
- Full featured, high-performance, low power, easy to use
- Delivered as a complete solution integrated and verified with the Mixel PHY

Conclusion

- The trend towards higher resolution, pixel depth and frame rate cameras and displays is driving the need for higher data rate interfaces.
- The MIPI Alliance Camera Serial Interface (CSI) and Display Serial Interface (DSI) standards are evolving to meet these needs.
- These trends will impact MIPI designs in several ways:
  - Higher I/O and clock rates, wider interfaces, use of multi-mode PHYs, use of data compression, etc.
- MIPI designers should consider these trends as they create their product roadmaps and associated designs.

For More Information

- Visit our exhibit in the Grand Hall during the conference.

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