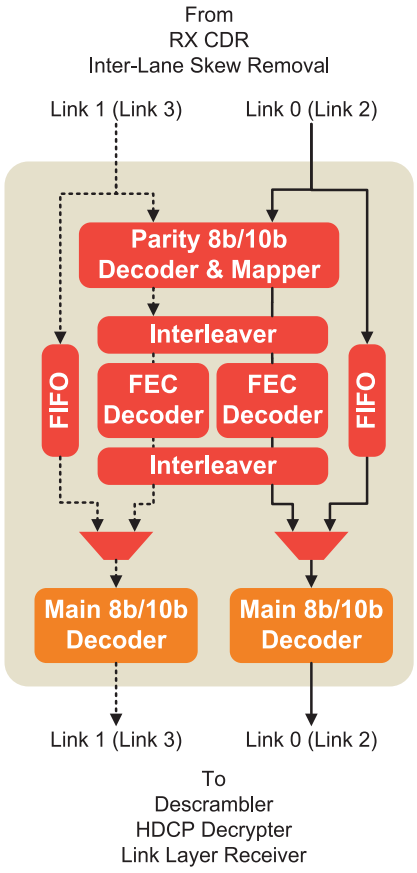
VESA DisplayPort 1.4 FEC RX IP Core

Applications

- UHD monitors
- DisplayPort 1.4 hubs & accessories
- USB Type-C hubs & accessories
- UHD TVs

Hardent DP1.4 FEC RX IP



Description

The DisplayPort™ Forward Error Correction (FEC) Receiver IP Core implements Reed-Solomon FEC and symbol interleaving as specified by the VESA DisplayPort 1.4 specification. Forward Error Correction is required to ensure glitch-free Display Stream Compression (DSC) bitstream transport.

Key Features

- VESA DisplayPort 1.4 compliant
- Reed Solomon RS (254,250) FEC, 10-bit symbols
- Two-way interleaving for 1-, 2- and 4-lane modes (4-lane mode requires 2 FEC IP core instances)
- Optionally includes the Main 8b/10b decoder
- Status and control can be done with signals or optionally via an integrated APB register module
- Single unified APB interface supports 4-lane mode
- Performance monitoring and statistics counters
- High level of error resiliency

Deliverables

- Encrypted RTL source code IP core
- Functional and structural coverage reports
- Comprehensive integration guide
- Technical support and maintenance updates

Product Options

- IP customization and integration services available on request
- Multi-project and perpetual licenses available
- UVM verification bindable modules

Hardent a Rambus company