VESA VDC-M 1.2 Encoder IP Core

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Incoming Pixels

Input De-multiplexer

VDC-M Encoder Hard Slice Instance #N

Buffers

N= 1, 2, 4, or 8

Slices Multiplexer

Display Transmitter(s)

VDC-M Compressed Bitstreams
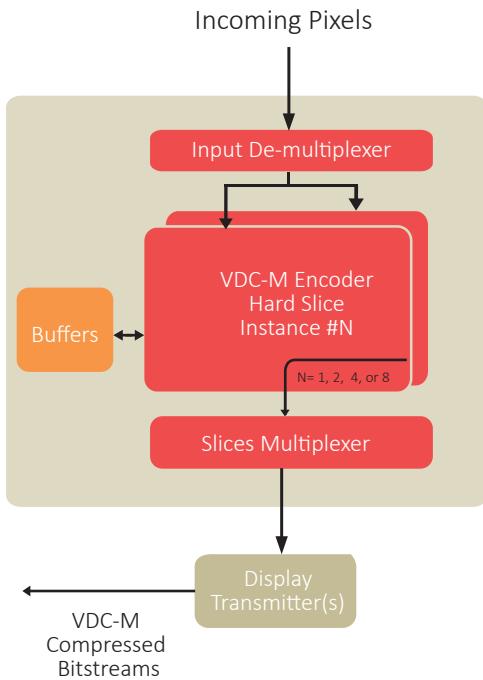
Description

The Hardent VESA VDC-M 1.2 Encoder IP Core implements a fully compliant VESA Display Compression-M (VDC-M) 1.2 encoder to deliver visually lossless video compression. The encoder supports various usage models, including typical MIPI Display Serial Interface 2 (MIPI DSI-2) usage models.

Key Features

- VESA Display Compression-M (VDC-M) 1.2 compliant
- Supports all VDC-M encoding mechanisms
    - o BP, transform, MPP, MPP fallback, and BP skip
    - o Flatness detection and signalling
- Configurable maximum display resolution of up to 16Kx16K
    - o Typical 4K (4096x2160), 5K UHD+, and 8K UHD supported
- Configurable compressed bit rate, in increments of 1/16 bits per pixel (bpp)
- 8, 10, or 12 bits per component video
- 4:4:4 sampling for RGB video input format
- 4:4:4, 4:2:2, and 4:2:0 sampling for YCbCr video input formats
- Parameterizable number of parallel slice encoder instances (1,2, 4, or 8) to adapt to the capability of the technology and target display resolutions used
- Supports logical slice encoding (soft slice) in each physical encoder (hard slice)
- Ultra-low latency
- Pixel throughput of two pixels per clock per hard slice encoder
- Optimized for power saving

Deliverables

- Encrypted RTL source code IP core
- Functional and structural coverage reports
- Comprehensive integration guide
- Technical support and maintenance updates

Product Options

- IP customization and integration services available
- Multi-project licenses available

Hardent

a *Rambus* company