Rambus

SerDes Interfaces

Optimized for power and area, our line-up of SerDes interface solutions deliver maximum performance and flexibility for today's most challenging systems.

Fully Standards-Compatible

- Faster time-to-market
- Multi-protocol support

Enhanced Design Flexibility

- Flexible packaging options
- Improved margin and yield

Reduced Power

- Wide range of PLL clock multipliers
- Fine-grain power-up/down options

Overview

Our SerDes interfaces are high-quality, complete solutions designed with a system-oriented approach to maximize flexibility and ease integration for our customers. Optimized for power and area at peak bandwidth, Rambus SerDes interfaces enable differentiation while maintaining compatibility with industry standards.

The SerDes interface family includes a range of solutions to meet a variety of speed and application requirements. The family of solutions includes:

Multi-protocol SerDes

- 32G SerDes PHY
- 32G MR SerDes PHY
- 32G C2C SerDes PHY
- 28G SerDes PHY
- 16G SerDes PHY
- 8G SerDes PHY

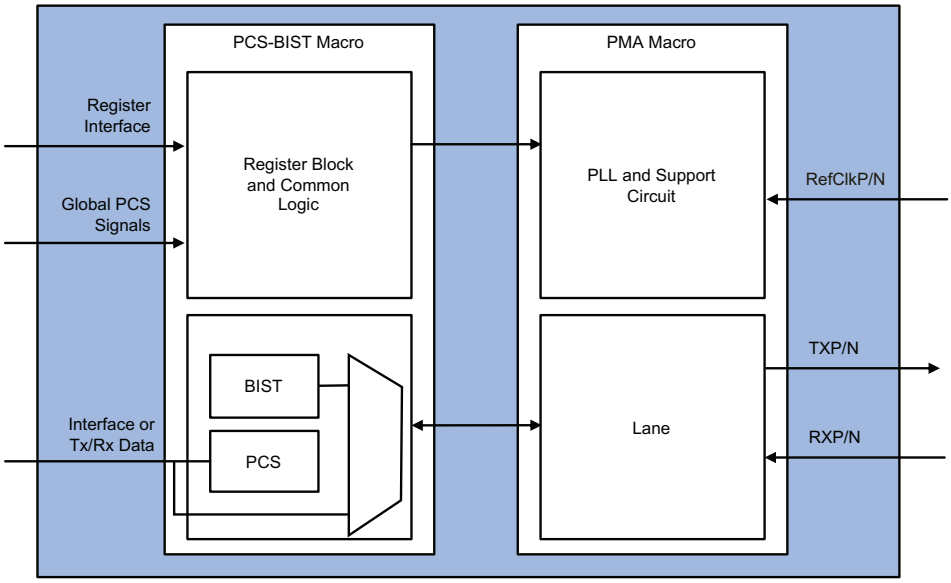
PCI Express®

- PCIe 6 PHY
- PCIe 5 PHY
- PCIe 4 PHY

Compute Express Link™

- CXL 3.0
- CXL 2.0
- CXL 1.1/1.0

Example SerDes PHY Configuration



We offer complete PHY solutions – our SerDes PHY includes a Physical Media Attachment (PMA) macro and Physical Coding Sub-layer with Built-in Self-Test (PCS-BIST) macro. The PHYs can also be configured to multiple channel widths and packaging options, which simplifies integration and maximizes design flexibility.

Features

- Available in 5nm, 7nm, 14nm, 28nm and 40nm FinFET process nodes
- PMA hard macros optimized for multiple protocols including PCIe, SATA, SAS, 400G/CEI/Interlaken, HMC, Fibre Channel and JESD204 interfaces
- Industry compliant PCS and MAC soft macros
- Support for x1, x2, x4 and x8 channel configurations
- Advanced Tx and Rx equalization
- Equalization adaptation
- BIST with PRBS generator and checker
- Data rate negotiation

Deliverables

PMA Hard Macro

- Verilog models
- LEF abstracts (.lef)
- Timing models (.lib)
- CDL netlists (.cdl)
- ATPG models
- IBIS-AMI models
- GDSII layout
- DRC and LVS reports
- PCS-BIST soft macro
- RTL model

Digital Controller

- Core (source code)
- Testbench (source code)

Datasheet

SoC Integration guide

Optional design integration and bring-up support services

rambus.com/serdes