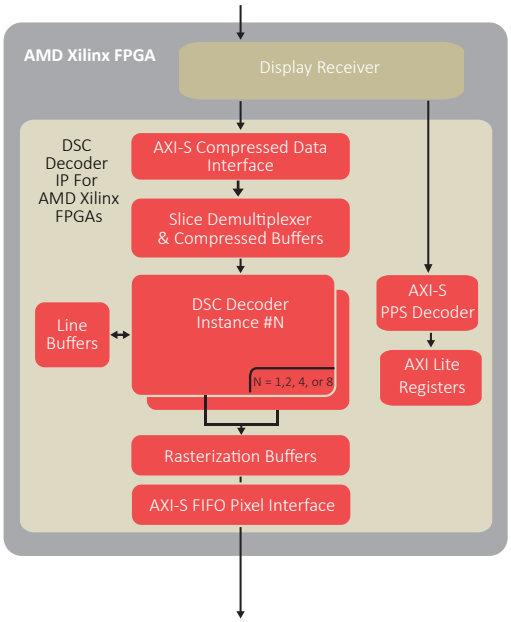
VESA DSC 1.2b Decoder IP Core for AMD Xilinx FPGAs

Applications

- 4K / 8K / UHD TVs & monitors
- AR / VR products
- DisplayPort™ 1.4 products
- USB Type-C products
- HDMI® 2.1 products

Hardent DSC Decoder IP For AMD Xilinx FPGAs



Key Features

- VESA® Display Stream Compression (DSC) 1.2b compliant
- Supports all DSC 1.2b mandatory and optional encoding mechanisms
- Backward compatible to DSC v1.1
- Configurable maximum display resolution up to 8K (FUHD)
- 8, 10, 12 bits per video component
- YCbCr and RGB video output format
- 4:4:4, 4:2:2, and 4:2:0 native coding
- Resilient to bitstream corruption
- 3 pixels / clock internal processing architecture in 4:4:4
- 6 pixels / clock internal processing architecture in 4:2:2 and 4:2:0
- Parameterizable number of parallel slice decoder instances (1, 2, 4, 8) to adapt to the capability of the technology and target display resolutions used
- Automatic run time configuration of the number of parallel slice decoder instances in use
- Support for AMD Xilinx® 7 Series, UltraScale™, and UltraScale+™ FPGAs
- AXI-S interfaces for easy integration in the Vivado® IP integrator
- AXI-Lite interface for register access
- PPS 128 bytes block decoding
- Compliant solution for DisplayPort 1.4 or HDMI 2.1
  - o Compatibility for slices per line requirements
- Supports flexible usage models and design architecture (inline decoding or panel frame buffer decoding)

Deliverables

- IP for AMD Xilinx Vivado Design Suite containing DSC Decoder core in netlist format, AXI-S Interface, and AXI-Lite Registers modules in RTL
- IP specification
- Comprehensive integration guide
- Technical support and maintenance updates
- Integration or design services available on request

Hardent a Rambus company