

VESA VDC-M 1.2

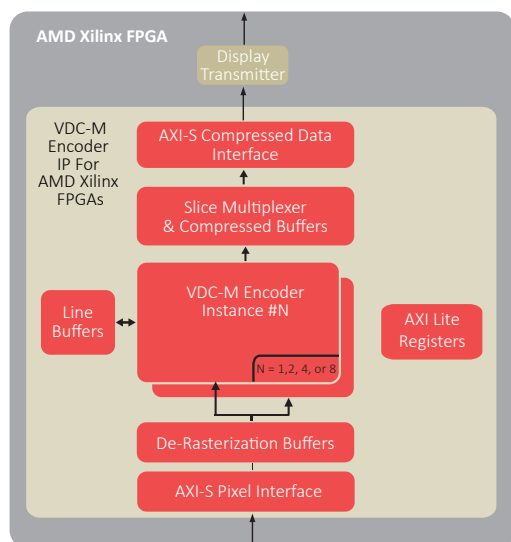
Encoder

IP Core for AMD Xilinx FPGAs

Applications

- 4K / 8K / UHD video sources
- MIPI DSI-2 products
- Test equipment
- Automotive video systems

Hardent VDC-M Encoder IP For AMD Xilinx FPGAs



Key Features

- VESA® Display Compression-M (VDC-M) 1.2 compliant
- Supports all VDC-M encoding mechanisms
 - BP, transform, MPP, MPP fallback, and BP skip
 - Flatness detection and signalling
- Configurable maximum display resolution of up to 16Kx16K
 - Typical 4K (4096x2160), 5K UHD+, and 8K UHD supported
- Configurable compressed bit rate, in increments of 1/16 bits per pixel (bpp)
- 8, 10, or 12 bits per component video
- 4:4:4 sampling for RGB video input format
- 4:4:4, 4:2:2, and 4:2:0 sampling for YCbCr video input formats
- Pixel throughput of two (2) pixels per clock per hard slice encoder
- Parameterizable number of parallel slice encoder instances (1, 2, 4, or 8) to adapt to the capability of the technology and target display resolutions used
- Logical slice encoding (2 soft slices) in each physical encoder (hard slice)
- Support for AMD Xilinx® UltraScale™ and UltraScale+™ FPGAs
- AXI-S interfaces for easy integration in the IP Vivado® integrator
- AXI-Lite interface for register access
- Compliant solution for MIPI® DSI-2™ v1.1
- Supports flexible usage models and design architecture

Deliverables

- IP for AMD Xilinx Vivado Design Suite containing VDC-M Encoder core in netlist format, AXI-S Interface, and AXI-Lite Registers modules in RTL
- IP specification
- Comprehensive integration guide
- Technical support and maintenance updates
- Integration or design services available on request